

TPS25200 5-V eFuse With Precision Adjustable Current Limit and Overvoltage Clamp

1 Features

- 2.5-V to 6.5-V Operation
- Input Withstands Up to 20 V
- 7.6-V Input Overvoltage Shutoff
- 5.25-V to 5.55-V Fixed Overvoltage Clamp
- 0.6- μ s Overvoltage Lockout Response
- 3.5- μ s Short Circuit Response
- Integrated 60-m Ω High-Side MOSFET
- Up to 2.5 A Continuous Load Current
- \pm 6% Current-Limit Accuracy at 2.9 A
- Reverse Current Blocking While Disabled
- Built-in Soft Start
- Pin-to-Pin Compatible with TPS2553
- UL 2367 Recognized
 - File No. 169910
 - $R_{ILIM} \geq 33 \text{ k}\Omega$ (3.12 A Maximum)

2 Applications

- USB Power Switch
- USB Slave Devices
- Cell/Smart Phones
- 3G, 4G Wireless Data-card
- Solid State Drives (SSD)
- 3-V or 5-V Adapter Powered Devices

3 Description

The TPS25200 is a 5-V eFuse with precision current limit and overvoltage clamp. The device provides robust protection for load and source during overvoltage and overcurrent events.

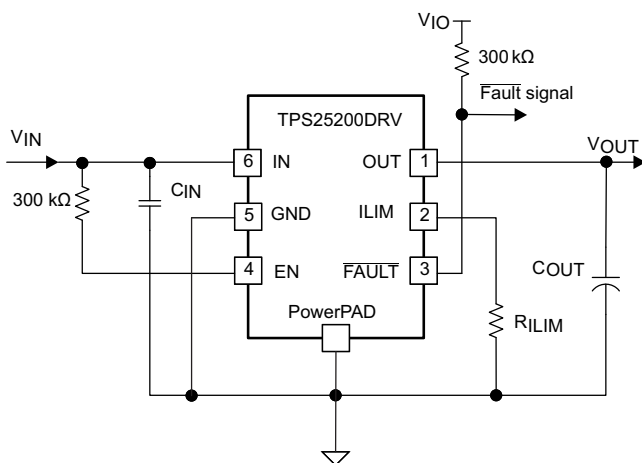
The TPS25200 is an intelligent protected load switch with V_{IN} tolerant to 20 V. In the event that an incorrect voltage is applied at IN, the output clamps to 5.4 V to protect the load. If the voltage at IN exceeds 7.6 V, the device disconnects the load to prevent damage to the device and/or load.

The TPS25200 has an internal 60-m Ω power switch and is intended for protecting source, device, and load under a variety of abnormal conditions. The device provides up to 2.5 A of continuous load current. Current limit is programmable from 85 mA to 2.9 A with a single resistor to ground. During overload events output current is limited to the level set by R_{ILIM} . If a persistent overload occurs the device eventually goes into thermal shutoff to prevent damage to the TPS25200.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS25200	SON (6)	2.00 mm x 2.00 mm

Simplified Schematic



V_{OUT} vs V_{IN}

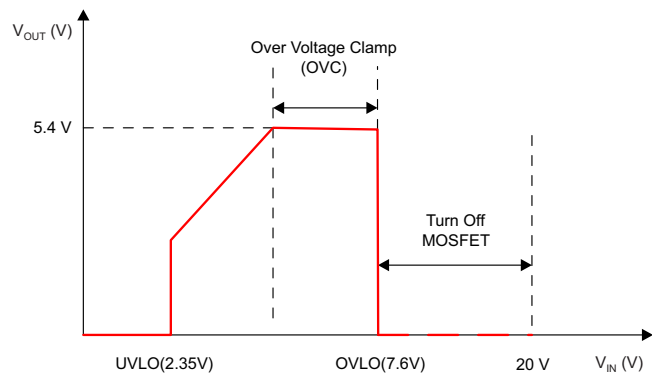


Table of Contents

1 Features	1	8.3 Feature Description	10
2 Applications	1	8.4 Device Functional Modes	12
3 Description	1	9 Application and Implementation	13
4 Revision History	2	9.1 Application Information	13
5 Pin Configuration and Functions	3	9.2 Typical Application	13
6 Specifications	4	10 Power Supply Recommendations	21
6.1 Absolute Maximum Ratings	4	11 Layout	21
6.2 ESD Ratings	4	11.1 Layout Guidelines	21
6.3 Recommended Operating Conditions	4	11.2 Layout Example	21
6.4 Thermal Information	4	12 Device and Documentation Support	22
6.5 Electrical Characteristics	5	12.1 Documentation Support	22
6.6 Timing Requirements	6	12.2 Receiving Notification of Documentation Updates	22
6.7 Typical Characteristics	7	12.3 Community Resources	22
7 Parameter Measurement Information	8	12.4 Trademarks	22
8 Detailed Description	9	12.5 Electrostatic Discharge Caution	22
8.1 Overview	9	12.6 Glossary	22
8.2 Functional Block Diagram	10	13 Mechanical, Packaging, and Orderable Information	22

4 Revision History

Changes from Revision A (March 2014) to Revision B

Page

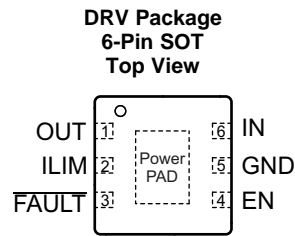
- | | |
|---|---|
| • Added UL certification status to Features section | 1 |
|---|---|

Changes from Original (March 2014) to Revision A

Page

- | | |
|--|----|
| • Changed the t_{off} TYP value From: 0.24 ms To: 0.22 ms | 6 |
| • Added condition: $V_{EN} = V_{IN} = 0$ V to Figure 3 | 7 |
| • Changed Figure 8 graph title From: Discharge Resistance To: V_{IN} | 7 |
| • Changed Equation 4 From = 2470 mA to = 2479 mA | 15 |

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Logic-level control input. When is driven high, the power switch is enabled. When it is driven low, turn power switch off. This pin cannot be left floating and it must be limited below the absolute maximum rating if tied to V_{IN}
$\overline{\text{FAULT}}$	3	O	Active-low open-drain output, asserted during overcurrent, overvoltage or overtemperature. Connect a pull up resistor to the logic I/O voltage
GND	5	—	Ground connection; connect externally to PowerPAD
ILIM	2	O	External resistor used to set current-limit threshold; Recommended $33\text{ k}\Omega \leq R_{ILIM} \leq 1100\text{ k}\Omega$
IN	6	I	Input voltage; connect a $0.1\text{-}\mu\text{F}$ or greater ceramic capacitor from IN to GND as close to the IC as possible
OUT	1	O	Protected power switch V_{OUT}
PowerPAD™	PAD	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND terminal externally

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Voltage on IN	-0.3	20	V
Voltage on OUT, EN, ILIM, $\overline{\text{FAULT}}$	-0.3	7	V
Voltage from IN to OUT	-7	20	V
I_O Continuous output current	Thermally Limited		
Continuous $\overline{\text{FAULT}}$ output sink current		25	mA
Continuous ILIM output source current		150	μA
T_J Operating junction temperature	Internally limited		
T_{stg} Storage temperature	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolutemaximum- rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

	VALUE	UNIT
$V_{\text{(ESD)}}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 500
		V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN} Input voltage of IN	2.5	6.5	V
V_{EN} Enable terminal voltage	0	6.5	V
$I_{\overline{\text{FAULT}}}$ Continuous $\overline{\text{FAULT}}$ sink current	0	10	mA
I_{OUT} Continuous output current of OUT		2.5	A
R_{ILIM} Current-limit set resistors	33	1100	$\text{k}\Omega$
T_J Operating junction temperature	-40	125	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TPS25200	UNIT
	DRV (SOT)	
	6 PINS	
θ_{JA} Junction-to-ambient thermal resistance	66.5	$^{\circ}\text{C}/\text{W}$
θ_{Jctop} Junction-to-case (top) thermal resistance	83.4	$^{\circ}\text{C}/\text{W}$
θ_{JB} Junction-to-board thermal resistance	36.1	$^{\circ}\text{C}/\text{W}$
ψ_{JT} Junction-to-top characterization parameter	1.6	$^{\circ}\text{C}/\text{W}$
ψ_{JB} Junction-to-board characterization parameter	36.5	$^{\circ}\text{C}/\text{W}$
θ_{Jcbot} Junction-to-case (bottom) thermal resistance	7.6	$^{\circ}\text{C}/\text{W}$

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Conditions are $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$ and $2.5\text{ V} \leq V_{\text{IN}} \leq 6.5\text{ V}$. $V_{\text{EN}} = V_{\text{IN}}$, $R_{\text{ILIM}} = 33\text{ k}\Omega$. Positive current into terminals. Typical value is at 25°C . All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER SWITCH							
$r_{\text{DS(on)}}$ IN–OUT resistance ⁽¹⁾		$2.5\text{ V} \leq V_{\text{IN}} \leq 5\text{ V}$, $I_{\text{OUT}} = 2.5\text{ A}$	$T_J = 25^{\circ}\text{C}$	60	70	m Ω	
			$-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$	60	90		
			$-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$	60	99		
ENABLE INPUT EN							
	EN terminal turnon threshold	Input rising			1.9	V	
	EN terminal turnoff threshold	Input falling	0.6			V	
	Hysteresis			330 ⁽²⁾		mV	
I_{EN}	Leakage current	$V_{\text{EN}} = 0\text{ V}$ or 5.5 V	–2		2	μA	
DISCHARGE							
R_{DCHG}	OUT discharge resistance	$V_{\text{OUT}} = 5\text{ V}$, $V_{\text{EN}} = 0\text{ V}$		480	625	Ω	
CURRENT LIMIT							
I_{OS}	Current - limit, See Figure 12	$R_{\text{ILIM}} = 33\text{ k}\Omega$		2773	2952	3127	mA
			$R_{\text{ILIM}} = 40.2\text{ k}\Omega$	2270	2423	2570	
			$R_{\text{ILIM}} = 56\text{ k}\Omega$	1620	1740	1860	
			$R_{\text{ILIM}} = 80.6\text{ k}\Omega$	1110	1206	1300	
			$R_{\text{ILIM}} = 150\text{ k}\Omega$	590	647	710	
			$R_{\text{ILIM}} = 1100\text{ k}\Omega$	40	83	130	
OVERVOLTAGE LOCKOUT, IN							
$V_{\text{(OVLO)}}$	IN rising OVLO threshold voltage	IN rising	6.8	7.6	8.45	V	
	Hysteresis			70 ⁽²⁾		mV	
VOLTAGE CLAMP, OUT							
$V_{\text{(OVC)}}$	OUT clamp voltage threshold	$C_L = 1\text{ }\mu\text{F}$, $R_L = 100\text{ }\Omega$, $V_{\text{IN}} = 6.5\text{ V}$	5.25	5.4	5.55	V	
SUPPLY CURRENT							
$I_{\text{IN(off)}}$	Supply current, low-level output	$V_{\text{EN}} = 0\text{ V}$, $V_{\text{IN}} = 5\text{ V}$		0.8	5	μA	
		$V_{\text{EN}} = 0$ or 5 V , $V_{\text{IN}} = 20\text{ V}$		1000	1700		
$I_{\text{IN(on)}}$	Supply current, high-level output	$V_{\text{IN}} = 5\text{ V}$, No load on OUT	$R_{\text{ILIM}} = 33\text{ k}\Omega$	143	200	μA	
			$R_{\text{ILIM}} = 150\text{ k}\Omega$	134	190		
I_{REV}	Reverse leakage current	$V_{\text{OUT}} = 6.5\text{ V}$, $V_{\text{IN}} = V_{\text{EN}} = 0\text{ V}$, $T_J = 25^{\circ}\text{C}$, measure I_{OUT}		3	5	μA	
UNDERVOLTAGE LOCKOUT, IN							
V_{UVLO}	IN rising UVLO threshold voltage	IN rising		2.35	2.45	V	
	Hysteresis			30 ⁽²⁾		mV	
FAULT FLAG							
V_{OL}	Output low voltage, $\overline{\text{FAULT}}$	$I_{\overline{\text{FAULT}}} = 1\text{ mA}$		50	180	mV	
	Off-state leakage	$V_{\overline{\text{FAULT}}} = 6.5\text{ V}$			1	μA	
THERMAL SHUTDOWN							
	Thermal shutdown threshold, OTSD2		155			$^{\circ}\text{C}$	
	Thermal shutdown threshold only in current-limit, OTSD1		135				
	Hysteresis			20 ⁽²⁾			

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.

(2) These parameters are provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

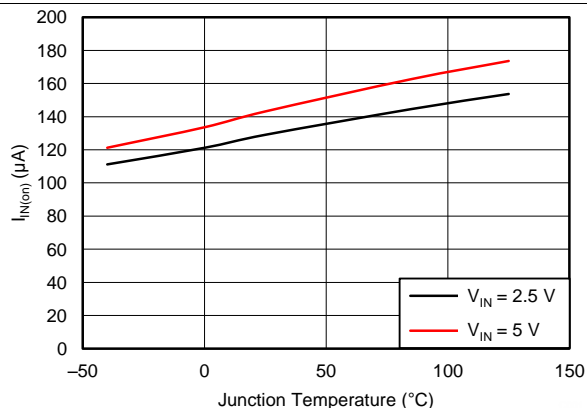
6.6 Timing Requirements

Conditions are $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$ and $2.5\text{ V} \leq V_{\text{IN}} \leq 6.5\text{ V}$. $V_{\text{EN}} = V_{\text{IN}}$, $R_{\text{ILIM}} = 33\text{ k}\Omega$. Positive current are into terminals. Typical value is at 25°C . All voltages are with respect to GND (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
t_r	OUT voltage rise time	$C_L = 1\ \mu\text{F}$, $R_L = 100\ \Omega$, (see Figure 10)		2.05	3.2	ms
t_f	OUT voltage fall time			0.18	0.2	
ENABLE INPUT EN						
t_{on}	Turnon time	$2.5\text{ V} \leq V_{\text{IN}} \leq 5\text{ V}$, $C_L = 1\ \mu\text{F}$, $R_L = 100\ \Omega$, (see Figure 10)		5.12	7.3	ms
t_{off}	Turnoff time			0.22	0.3	ms
CURRENT LIMIT						
$t_{(\text{IOS})}$	Short-circuit response time	$V_{\text{IN}} = 5\text{ V}$ (see Figure 12)		3.5 ⁽¹⁾		μs
OVERVOLTAGE LOCKOUT, IN						
$t_{(\text{OVLO_off_delay})}$	Turnoff delay for OVLO	$V_{\text{IN}} 5\text{ V to } 10\text{ V}$ with $1\text{-V}/\mu\text{s}$ ramp up rate, V_{OUT} with $100\text{-}\Omega$ load		0.6 ⁽¹⁾		μs
FAULT FLAG						
	$\overline{\text{FAULT}}$ deglitch	$\overline{\text{FAULT}}$ assertion or de-assertion due to overcurrent condition		5	8	12 ms

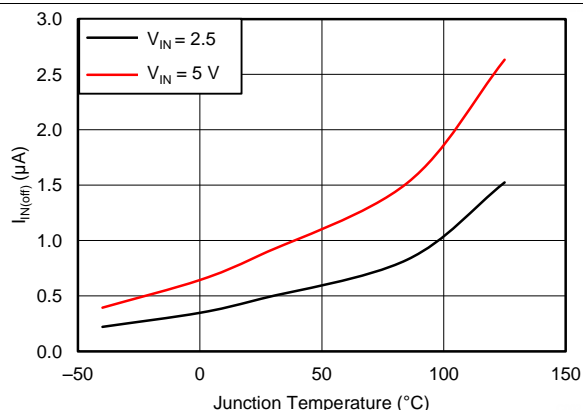
(1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.7 Typical Characteristics



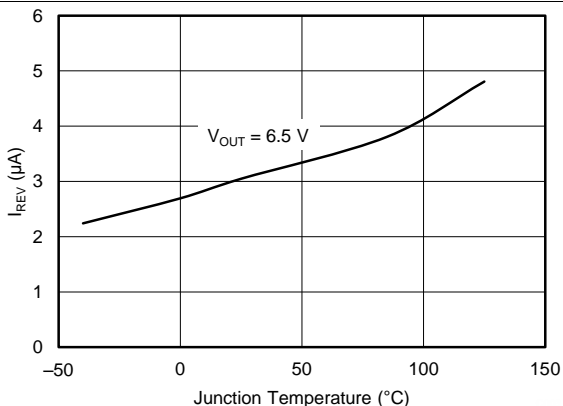
$R_{LIM} = 33\text{ K}\Omega$

Figure 1. $I_{IN(on)}$ vs Junction Temperature



$R_{LIM} = 33\text{ K}\Omega$

Figure 2. $I_{IN(off)}$ vs Junction Temperature



$V_{EN} = V_{IN} = 0\text{ V}$

Figure 3. I_{REV} vs Junction Temperature

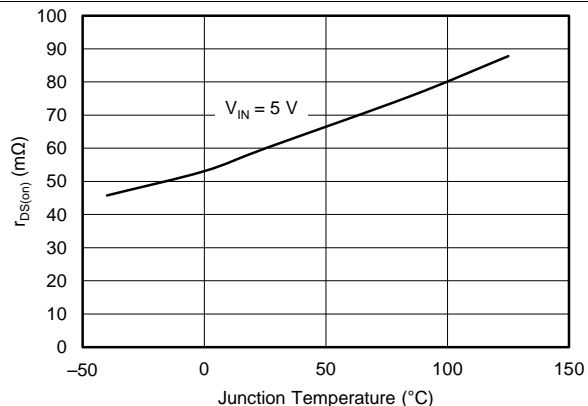
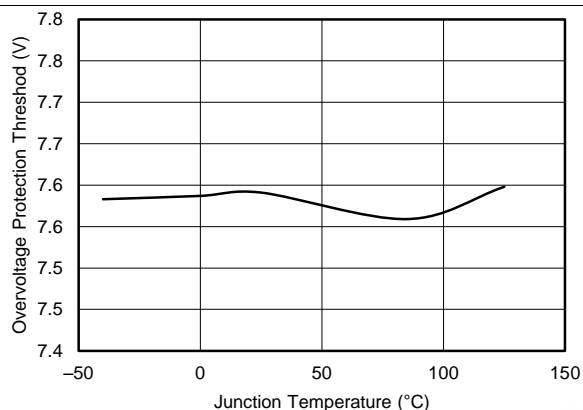
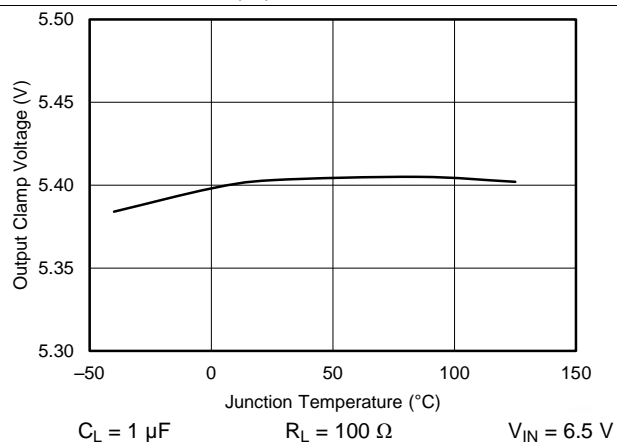


Figure 4. $r_{DS(on)}$ vs Junction Temperature



$V_{EN} = V_{IN} = 0\text{ V}$

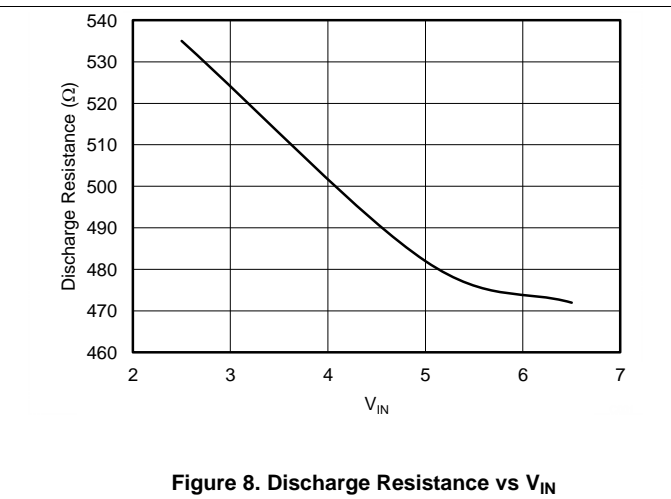
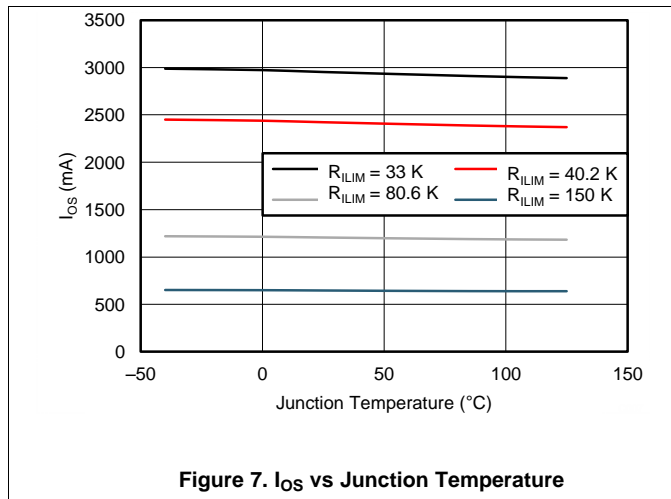
Figure 5. $V_{OV(LO)}$ vs Junction Temperature



$C_L = 1\ \mu\text{F}$ $R_L = 100\ \Omega$ $V_{IN} = 6.5\text{ V}$

Figure 6. $V_{O(VC)}$ vs Junction Temperature

Typical Characteristics (continued)



7 Parameter Measurement Information

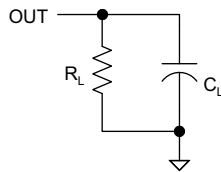


Figure 9. Output Rise-Fall Test Load

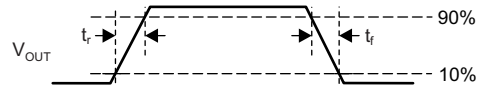


Figure 10. Power-On and Off Timing

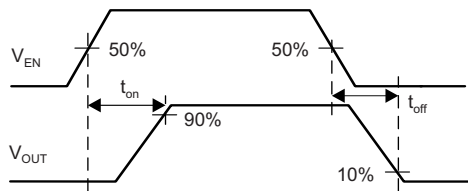


Figure 11. Enable Timing, Active High Enable

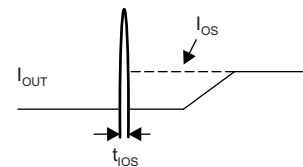


Figure 12. Output Short Circuit Parameters

8 Detailed Description

8.1 Overview

The TPS25200 is an intelligent low voltage switch or e-Fuse with robust overcurrent and overvoltage protection which are suitable for a variety of applications.

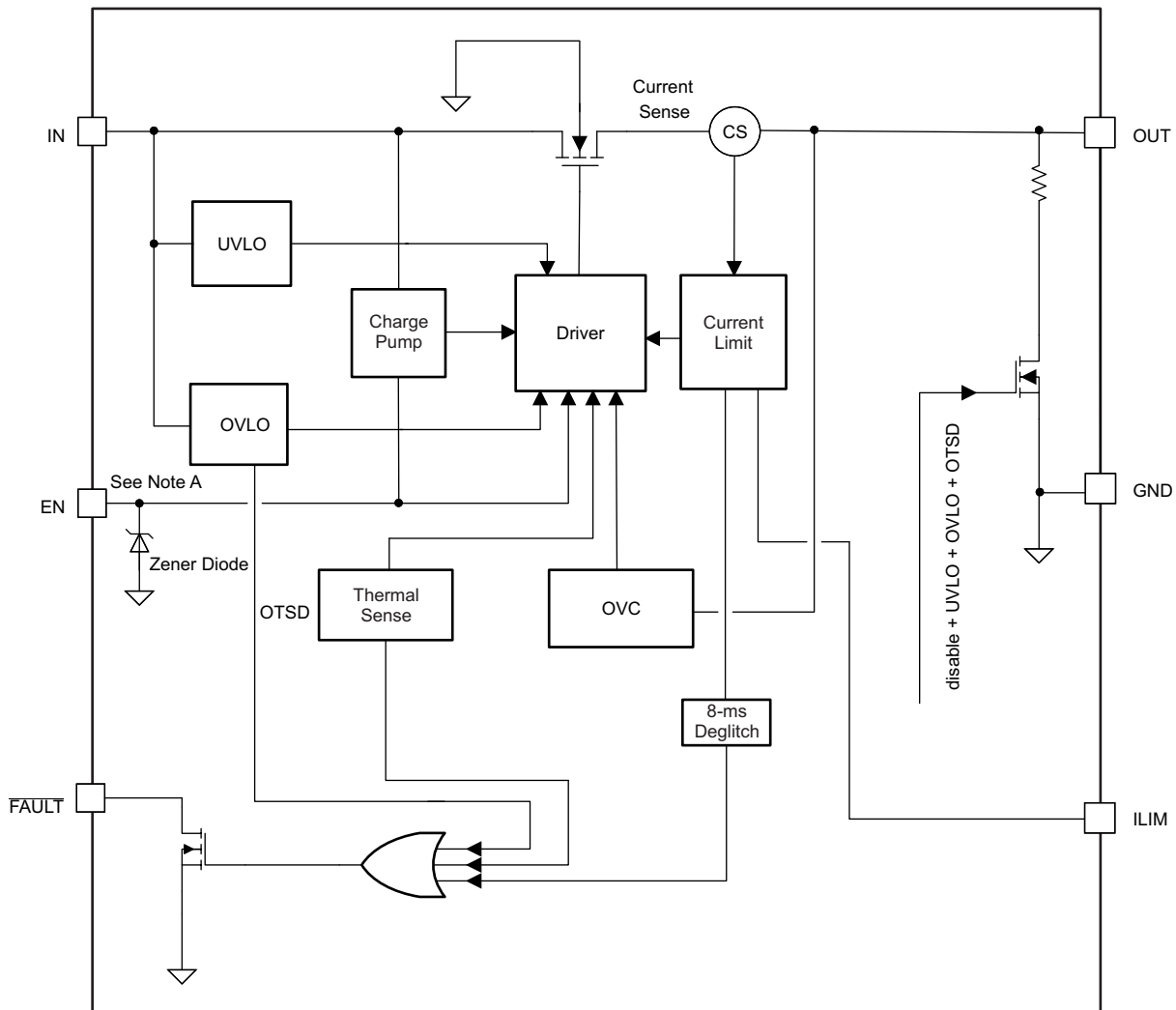
The TPS25200 current limited power switch uses N-channel MOSFETs in applications requiring up to 2.5 A of continuous load current. The device allows the user to program the current-limit threshold between 85 mA and 2.9 A (typical) via an external resistor. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS25200 Input can withstand 20-V DC voltage, but clamps V_{OUT} to a precision regulated 5.4 V and shuts down in the event V_{IN} exceeds 7.6 V. The device also integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply while the fast response short circuit protection isolates the load when a short circuit is detected.

The additional features include:

- Enable the device can be put into a sleep mode for portable applications.
- Overtemperature protection to safely shutdown in the event of an overcurrent event or a slight overvoltage event where the V_{OUT} clamp is engaged over an extended period of time.
- Deglitched fault reporting to filter the Fault signal to ensure the TPS25200 do not provide false fault alerts.
- Output discharge pull-down to help ensure a load is in fact off and not in some undefined operational state.
- Reverse blocking when disabled to prevent back-drive from an active load inadvertently causing undetermined behavior in the application.

8.2 Functional Block Diagram



A. 6.4-V Typical Clamp Voltage

8.3 Feature Description

8.3.1 Enable

This logic enable input controls the power switch and device supply current. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

EN can be tied to V_{IN} with a pull up resistor, and is protected with an integrated zener diode. Use a sufficiently large (300-k Ω) pull up resistor to ensure that the $V_{(EN)}$ is limited below the absolute maximum rating.

8.3.2 Thermal Sense

The TPS25200 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS25200 device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (minimum) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

Feature Description (continued)

The TPS25200 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (minimum) regardless of whether the power switch is in current limit and turns on the power switch after the device has cooled approximately 20°C. The TPS25200 continues to cycle off and on until the fault is removed.

8.3.3 Overcurrent Protection

The TPS25200 thermally protects itself by thermal cycling during an extended overcurrent condition. The device turns off when the junction temperature exceeds 135°C (typical) while in current limit. The device remains off until the junction temperature cools 20°C (typical) and then restarts. The TPS25200 cycles on/off until the overload is removed (see [Figure 26](#) and [Figure 29](#)).

The TPS25200 responds to an overcurrent condition by limiting their output current to the I_{OS} levels shown in [Figure 12](#). When an overcurrent condition is detected, the device maintains a constant output current and the output voltage is reduced accordingly. During an over current event, two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS25200 ramps the output current to I_{OS} . The TPS25200 devices limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see [Figure 12](#)). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to I_{OS} . Similar to the previous case, the TPS25200 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

8.3.4 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or overvoltage condition. The TPS25200 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS25200 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (8-ms typical) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an overtemperature event.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled into OVLO or out of OVLO. The TPS25200 does not assert the $\overline{\text{FAULT}}$ during output voltage clamp mode.

Connect $\overline{\text{FAULT}}$ with a pull up resistor to a low voltage I/O rail.

8.3.5 Output Discharge

A 480- Ω (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS25200 is in UVLO, disabled or OVLO. The pull down capability decreases as V_{IN} decreases ([Figure 8](#)).

8.4 Device Functional Modes

The TPS25200 V_{IN} can withstand up to 20 V. Within 0 V to 20 V range, it can be divided to four modes as shown in Figure 13.

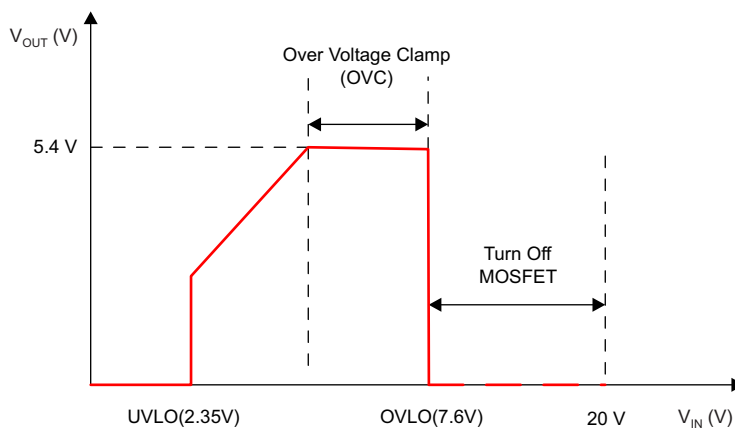


Figure 13. Output vs Input Voltage

8.4.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on and off cycling due to input voltage droop during turnon.

8.4.2 Overcurrent Protection (OCP)

When $2.35\text{ V} < V_{IN} < 5.4\text{ V}$, the TPS25200 is a traditional power switch, providing overcurrent protection.

8.4.3 Overvoltage Clamp (OVC)

When $5.4\text{ V} < V_{IN} < 7.6\text{ V}$, the overvoltage clamp (OVC) circuit clamps the output voltage to 5.4 V. Within this V_{IN} range, the overcurrent protection remains active.

8.4.4 Overvoltage Lockout (OVLO)

When V_{IN} exceeds 7.6 V, the overvoltage lockout (OVLO) circuit turns off the protected power switch.

9 Application and Implementation

9.1 Application Information

The TPS25200 is a 5-V eFuse with precision current limit and over-voltage clamp. When a slave device such as a mobile data-card device is hot plugged into a USB port as shown in Figure 14, an input transient voltage could damage the slave device due to the cable inductance. Placing the TPS25200 at the input of mobile device as over-voltage and overcurrent protector can safeguard these slave devices. Input transients also occur when the current through the cable parasitic inductance changes abruptly. This can occur when the TPS25200 turns off the internal MOSFET in response to an overvoltage or overcurrent event. The TPS25200 can withstand the transient without a bypass bulk capacitor, or other external overvoltage protection components at input side. The TPS25200 also can be used at host side as a traditional power switch pin-to-pin compatible with the TPS2553.

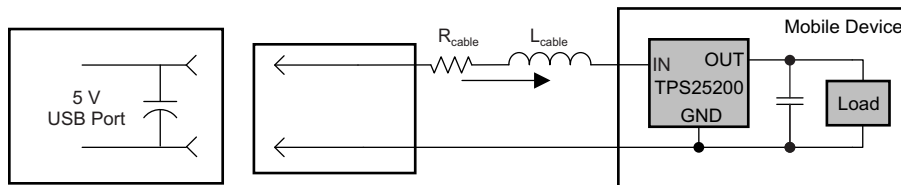


Figure 14. Hot Plug Into 5V USB port with Parasitic Cable Resistance and Inductance

9.2 Typical Application

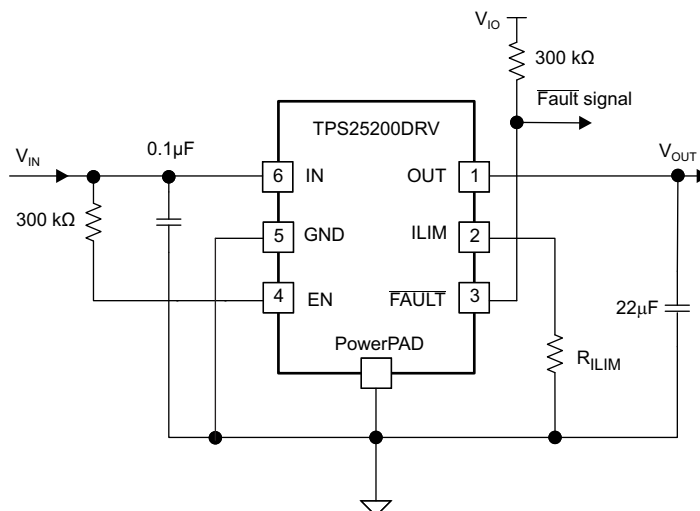


Figure 15. Overvoltage and Overcurrent Protector—Typical Application Schematic

Use the I_{OS} in the [Electrical Characteristics](#) table or I_{OS} in [Equation 1](#) to select the R_{ILIM} .

9.2.1 Design Requirements

For this design example, use the design parameters in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Normal input operation voltage	5 V
Output transient voltage	6.5 V
Minimum current limit	2.1 A
Maximum current limit	2.9 A

9.2.2 Detailed Design Procedure

9.2.2.1 Step by Step Design Produce

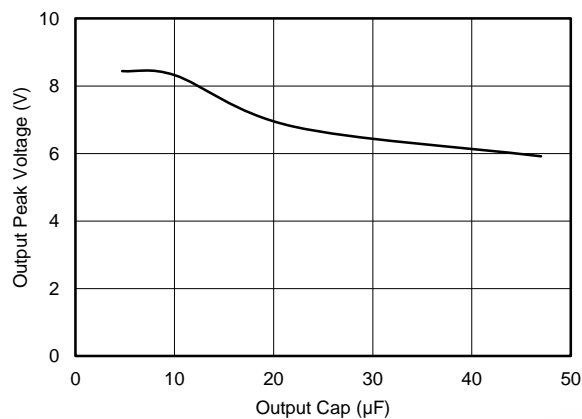
To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Output transient voltage
- Minimum Current Limit
- Maximum Current Limit

9.2.2.2 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, a 0.1- μF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

When V_{IN} ramp up exceed 7.6 V, V_{OUT} follows V_{IN} until the TPS25200 turns off the internal MOSFET after $t_{(\text{OVLO_off_delay})}$. Since $t_{(\text{OVLO_off_delay})}$ largely depends on the V_{IN} ramp rate, V_{OUT} sees some peak voltage. Increasing the output capacitance can lower the output peak voltage as shown in Figure 16.



**Figure 16. V_{OUT} Peak Voltage vs C_{OUT}
(V_{IN} Step From 5 V to 15 V with 1-V/ μs Ramp Up Rate)**

9.2.2.3 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS25200 uses an internal regulation loop to provide a regulated voltage on the ILIM terminal. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is $33 \text{ k}\Omega \leq R_{\text{ILIM}} \leq 1100 \text{ k}\Omega$ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM} . The current-limit threshold equations (IOS) in Equation 1 approximate the resulting overcurrent threshold for a given external resistor value R_{ILIM} . See the [Electrical Characteristics](#) table for specific current limit settings. The traces routing the R_{ILIM} resistor to the TPS25200 must be as short as possible to reduce parasitic effects on the current-limit accuracy.

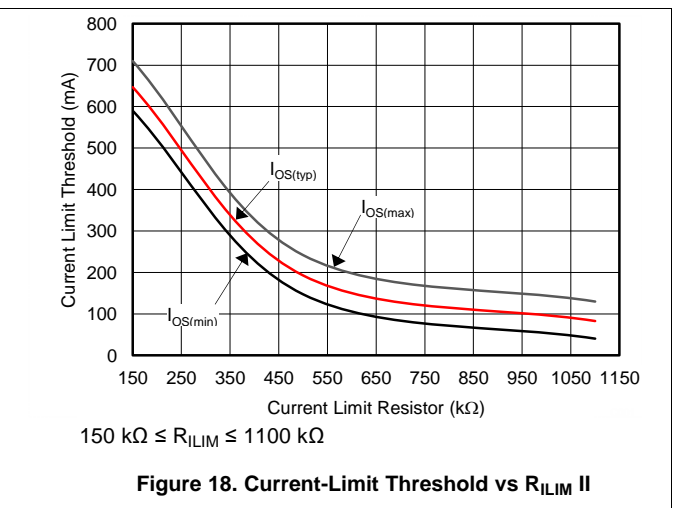
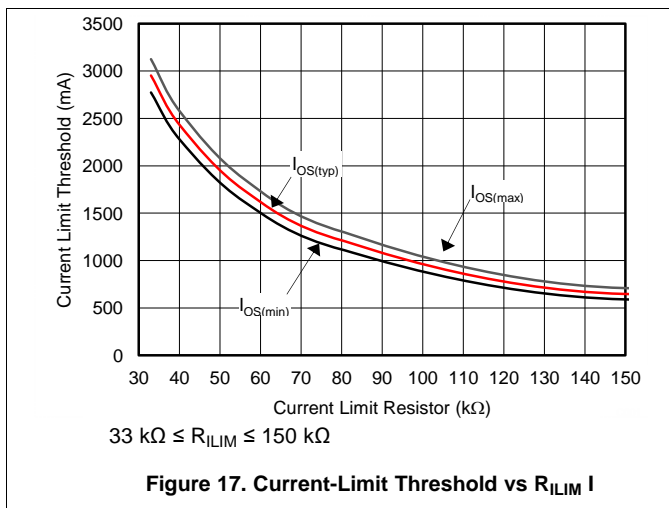
R_{ILIM} can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{\text{OS}(\text{min})}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{\text{OS}(\text{max})}$ curve.

To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve. See [Figure 17](#) and [Figure 18](#).

$$\begin{aligned}
 I_{OSmax}(mA) &= \frac{96754V}{R_{ILIM} \cdot 0.985k\Omega} + 30 \\
 I_{OSnom}(mA) &= \frac{98322V}{R_{ILIM} \cdot 1.003k\Omega} \\
 I_{OSmin}(mA) &= \frac{97399}{R_{ILIM} \cdot 1.015k\Omega} - 30
 \end{aligned}
 \tag{1}$$

Where $33\text{ k}\Omega \leq R_{ILIM} \leq 1100\text{ k}\Omega$.



9.2.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2.1 A must be delivered to the load so that the minimum desired current-limit threshold is 2100 mA. Use the I_{OS} equations ([Equation 1](#)) and [Figure 17](#) to select R_{ILIM} as shown in [Equation 2](#).

$$\begin{aligned}
 I_{OSmin}(mA) &= 2100\text{ mA} \\
 I_{OSmin}(mA) &= \frac{97399V}{R_{ILIM} \cdot 1.015k\Omega} - 30 \\
 R_{ILIM}(k\Omega) &= \left(\frac{97399}{I_{OS(min)} + 30} \right)^{\frac{1}{1.015}} = \left(\frac{97399}{2100 + 30} \right)^{\frac{1}{1.015}} = 43.22\text{ k}\Omega
 \end{aligned}
 \tag{2}$$

Select the closest 1% resistor less than the calculated value: $R_{ILIM} = 42.2\text{ k}\Omega$. This sets the minimum current-limit threshold at 2130 mA as shown in [Equation 3](#).

$$I_{OSmin}(mA) = \frac{97399V}{R_{ILIM} \cdot 1.015k\Omega} - 30 = \frac{97399}{(42.2 \times 1.01)^{1.015}} - 30 = 2130\text{mA}
 \tag{3}$$

Use the I_{OS} equations ([Equation 1](#)), [Figure 17](#), and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold as shown in [Equation 4](#).

$$I_{OSmax}(\text{mA}) = \frac{96754}{R_{ILIM}^{0.985}} + 30$$

$$I_{OSmax}(\text{mA}) = \frac{96754}{(42.2 \times 0.99)^{0.985}} + 30 = 2479 \text{ mA} \quad (4)$$

The resulting current-limit threshold minimum is 2130 mA and maximum is 2479 mA with $R_{ILIM} = 42.2\text{k}\Omega \pm 1\%$.

9.2.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 2.9 A must be delivered to the load so that the minimum desired current-limit threshold is 2900 mA. Use the I_{OS} equations (Equation 1) and Figure 18 to select R_{ILIM} as shown in Equation 5.

$$I_{OSmax}(\text{mA}) = 2900\text{mA}$$

$$I_{OSmax}(\text{mA}) = \frac{96754}{R_{ILIM}^{0.985} \text{ k}\Omega} + 30$$

$$R_{ILIM}(\text{k}\Omega) = \left(\frac{96754}{I_{OS(max)} - 30} \right)^{\frac{1}{0.985}} = \left(\frac{96754}{2900 - 30} \right)^{\frac{1}{0.985}} = 35.57 \text{ k}\Omega \quad (5)$$

Select the closest 1% resistor greater than the calculated value: $R_{ILIM} = 36 \text{ k}\Omega$. This sets the maximum current-limit threshold at 2894 mA as shown in Equation 6.

$$I_{OSmax}(\text{mA}) = \frac{96754\text{V}}{R_{ILIM}^{0.985} \text{ k}\Omega} + 30 = \frac{96754}{(36 \times 0.99)^{0.985}} + 30 = 2894\text{mA} \quad (6)$$

Use the I_{OS} equations, Figure 18, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold as shown in Equation 7.

$$I_{OSmin}(\text{mA}) = \frac{97399}{R_{ILIM}^{1.015}} - 30$$

$$I_{OSmin}(\text{mA}) = \frac{97399}{(36 \times 1.01)^{1.015}} - 30 = 2508\text{mA} \quad (7)$$

The resulting minimum current-limit threshold minimum is 2592 mA and maximum is 2894 mA with $R_{ILIM} = 36 \text{ k}\Omega \pm 1\%$.

9.2.2.6 Power Dissipation and Junction Temperature

The low on-resistance of the internal N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. When V_{IN} is lower than $V_{(OVC)}$, the TPS2500 is an traditional power switch. Using this value, the power dissipation can be calculated by using [Equation 8](#).

$$P_D = r_{DS(on)} \times I_{OUT}^2 \quad (8)$$

When V_{IN} exceed $V_{(OVC)}$, but lower than $V_{(OVLO)}$, the TPS25200 clamp output to fixed $V_{(OVC)}$, the power dissipation can be calculated by using [Equation 9](#).

$$P_D = (V_{IN} - V_{(OVC)}) \times I_{OUT}$$

where

- P_D = Total power dissipation (W)
 - $r_{DS(on)}$ = Power switch on-resistance (Ω)
 - $V_{(OVC)}$ = Overvoltage clamp voltage (V)
 - I_{OUT} = Maximum current-limit threshold (A)
- (9)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature using [Equation 10](#).

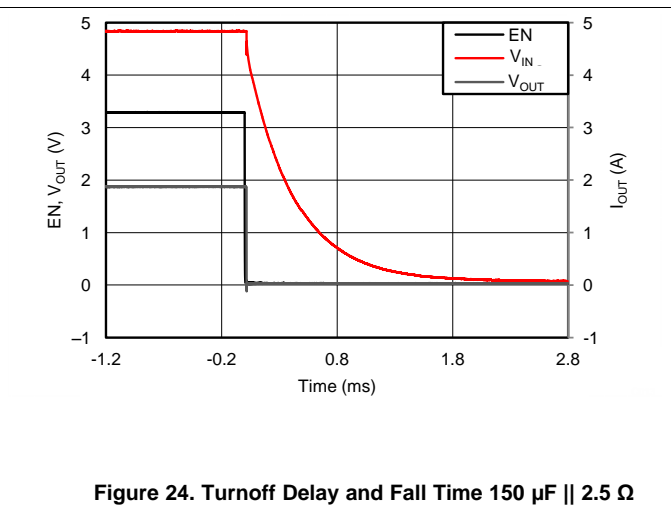
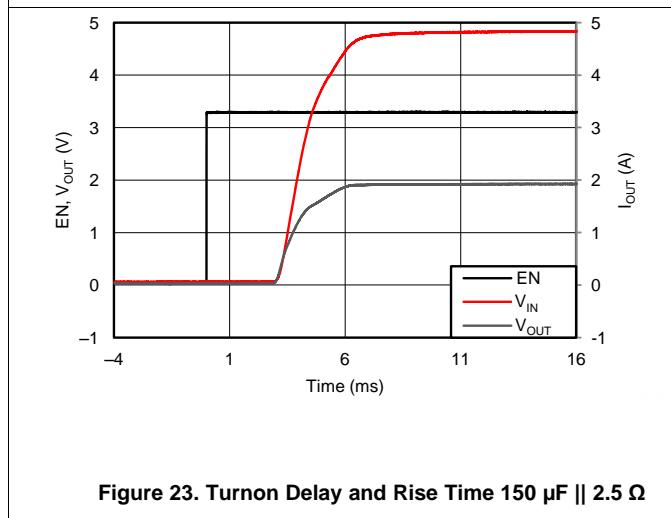
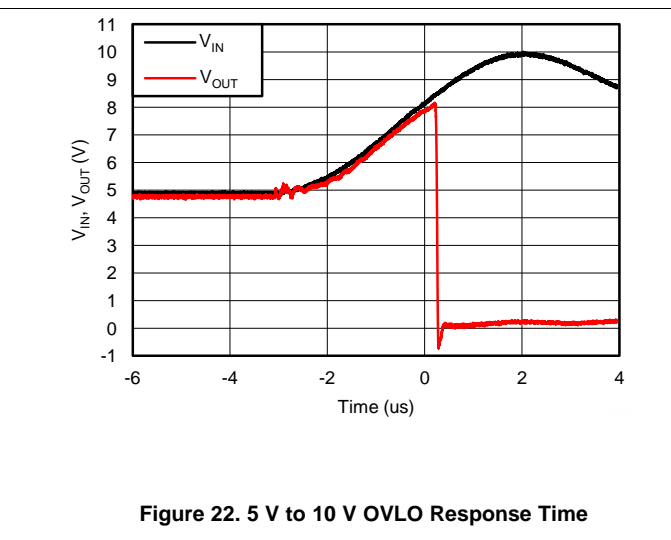
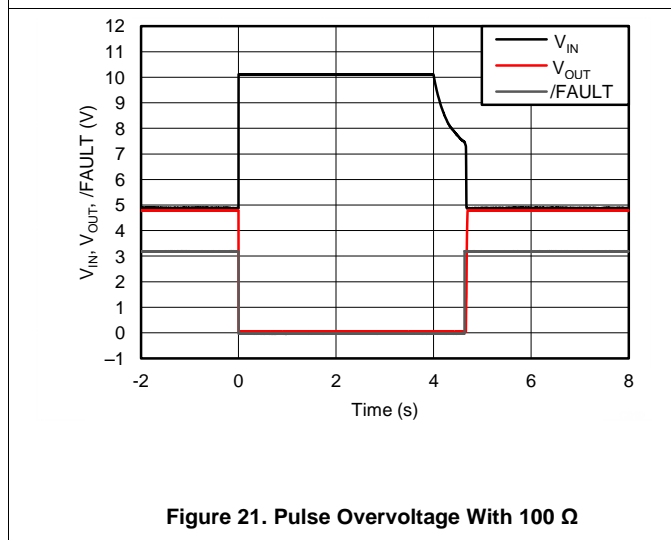
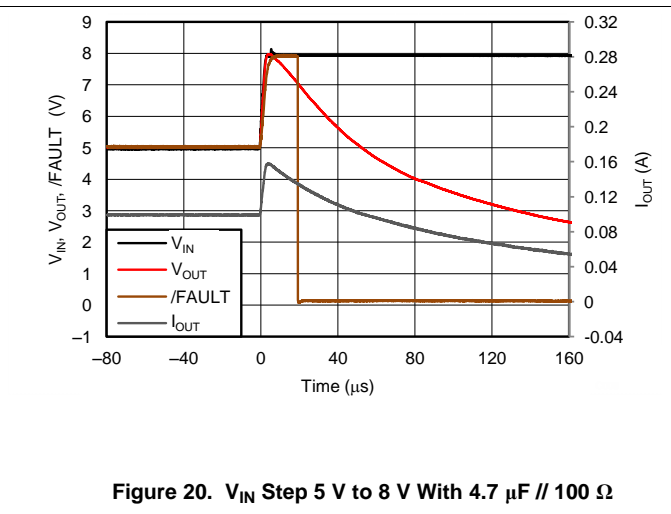
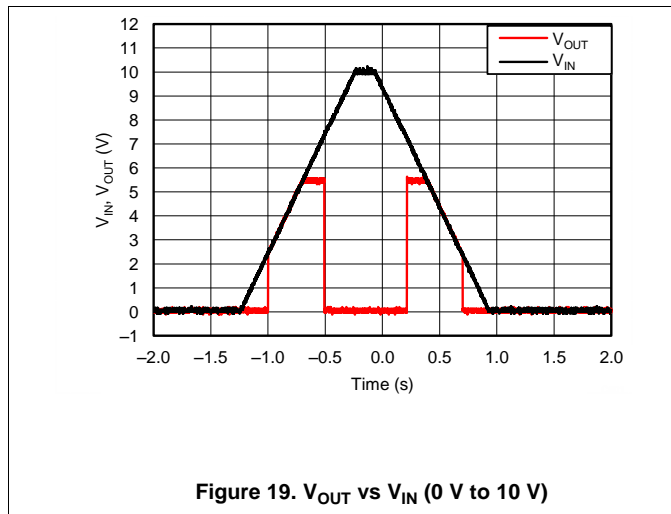
$$T_J = P_D \times \theta_{JA} + T_A$$

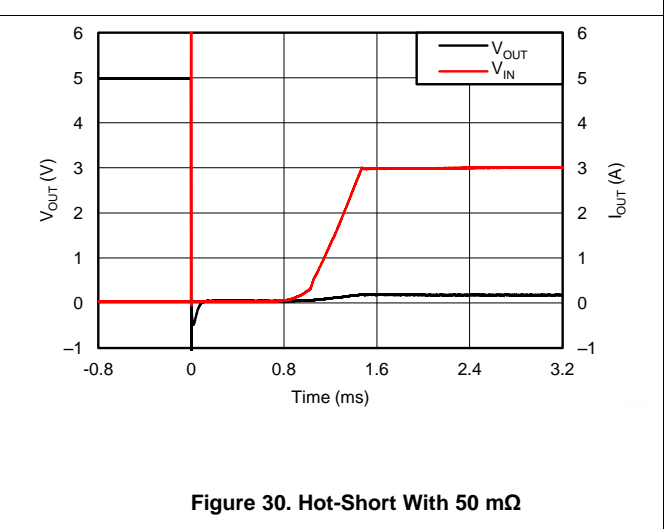
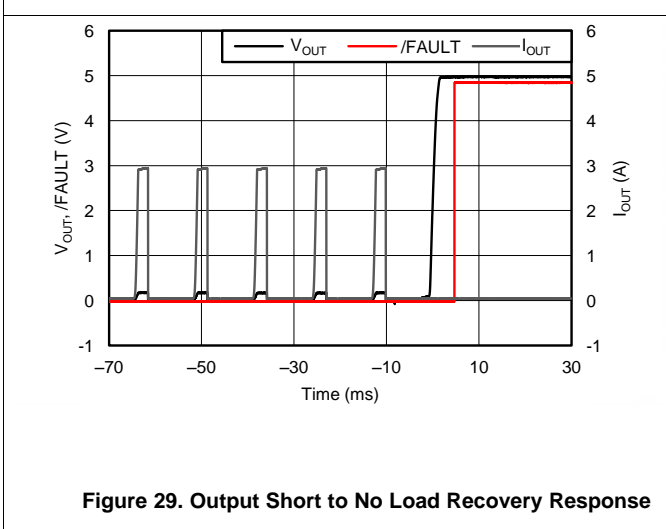
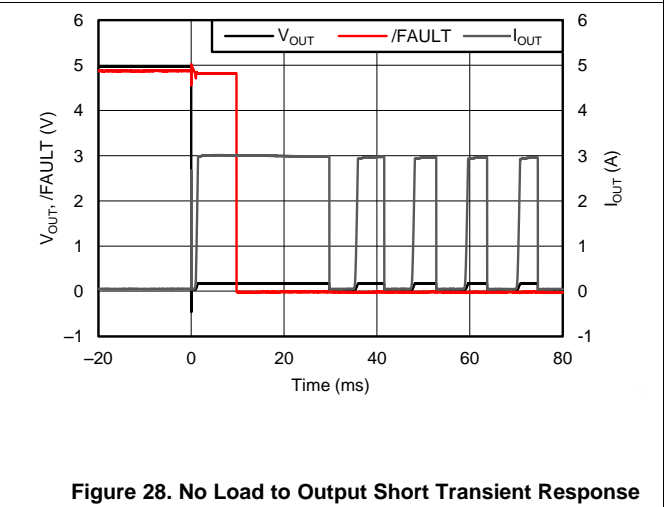
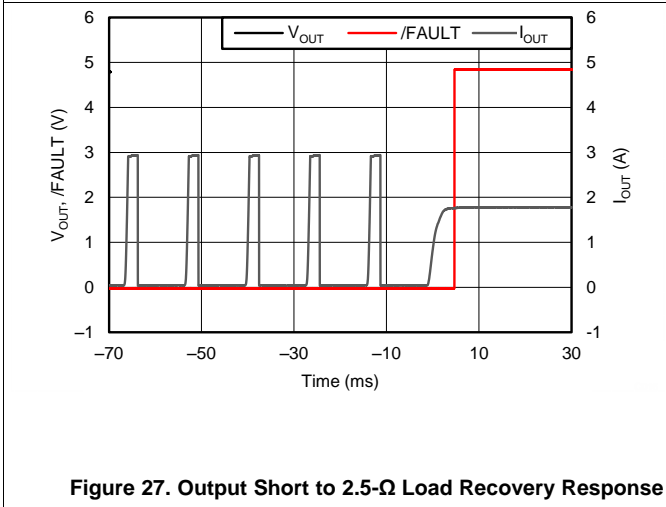
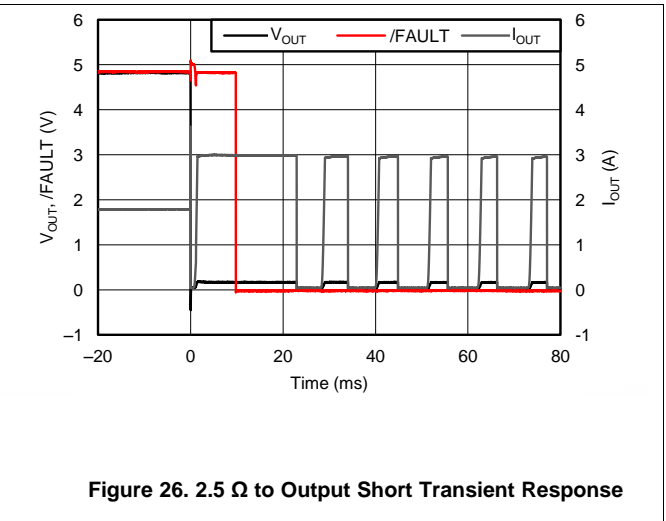
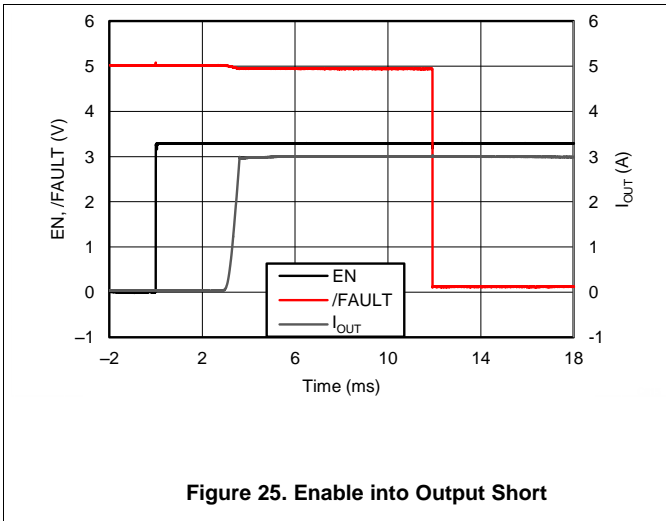
where

- T_A = Ambient temperature ($^{\circ}\text{C}$)
 - θ_{JA} = Thermal resistance ($^{\circ}\text{C}/\text{W}$)
 - P_D = Total power dissipation (W)
- (10)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA} , and thermal resistance is highly dependent on the individual package and board layout.

9.2.3 Application Curves





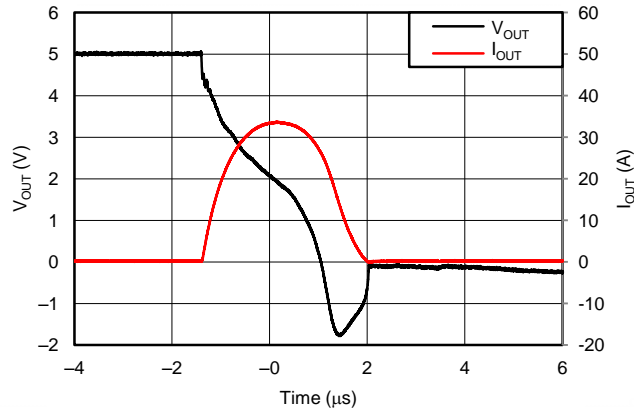


Figure 31. 50-mΩ Hot-Short Response Time

10 Power Supply Recommendations

The TPS25200 is designed for $2.7\text{ V} < V_{IN} < 5\text{ V}$ (typical) voltage rails. While there is a V_{OUT} clamp, it is not intended to be used to regulate V_{OUT} at approximately 5.4 V with $6\text{ V} < V_{IN} < 7\text{ V}$. This is a protection feature only.

11 Layout

11.1 Layout Guidelines

- For all applications, a 0.1- μF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.
- For output capacitance, refer to [Figure 16](#), low ESR ceramic cap is recommended.
- The traces routing the R_{ILIM} resistor to the device must be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

11.2 Layout Example

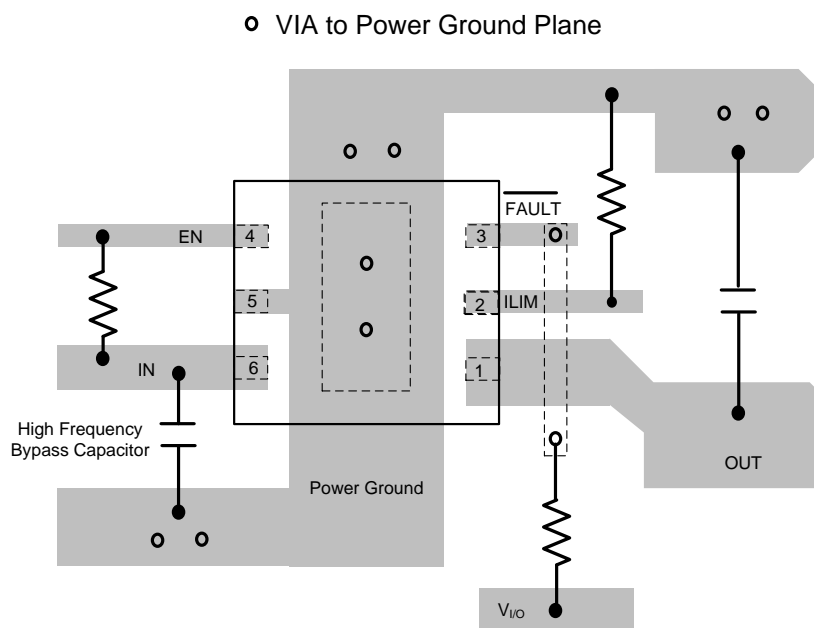


Figure 32. TPS25200 Board Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

[TPS25200 EVM User's Guide](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25200DRVR	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB	Samples
TPS25200DRVT	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS25200 :

- Automotive: [TPS25200-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25200DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS25200DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

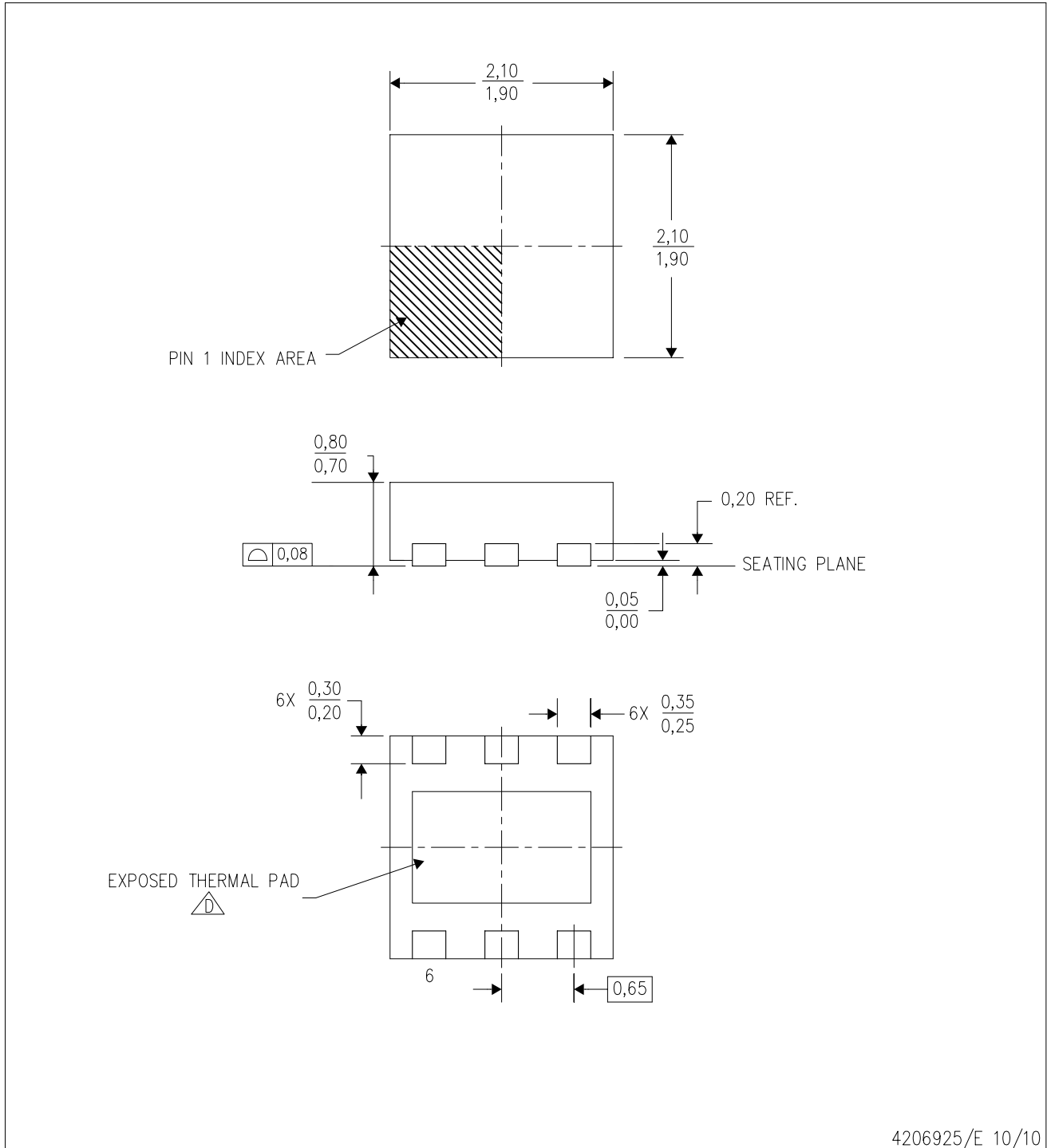

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25200DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS25200DRVT	WSON	DRV	6	250	205.0	200.0	33.0


MECHANICAL DATA

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

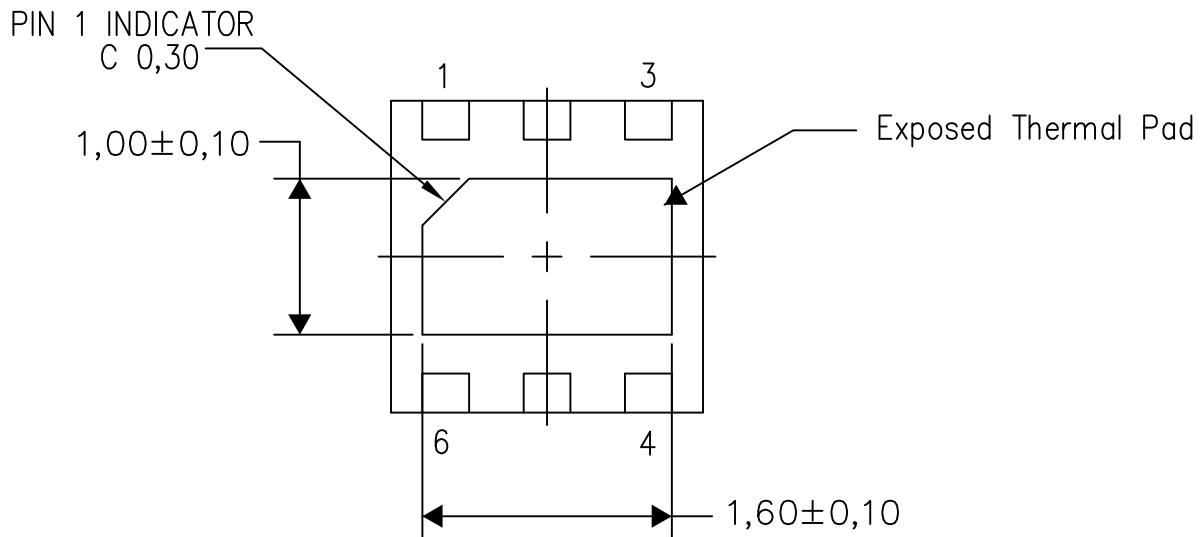
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

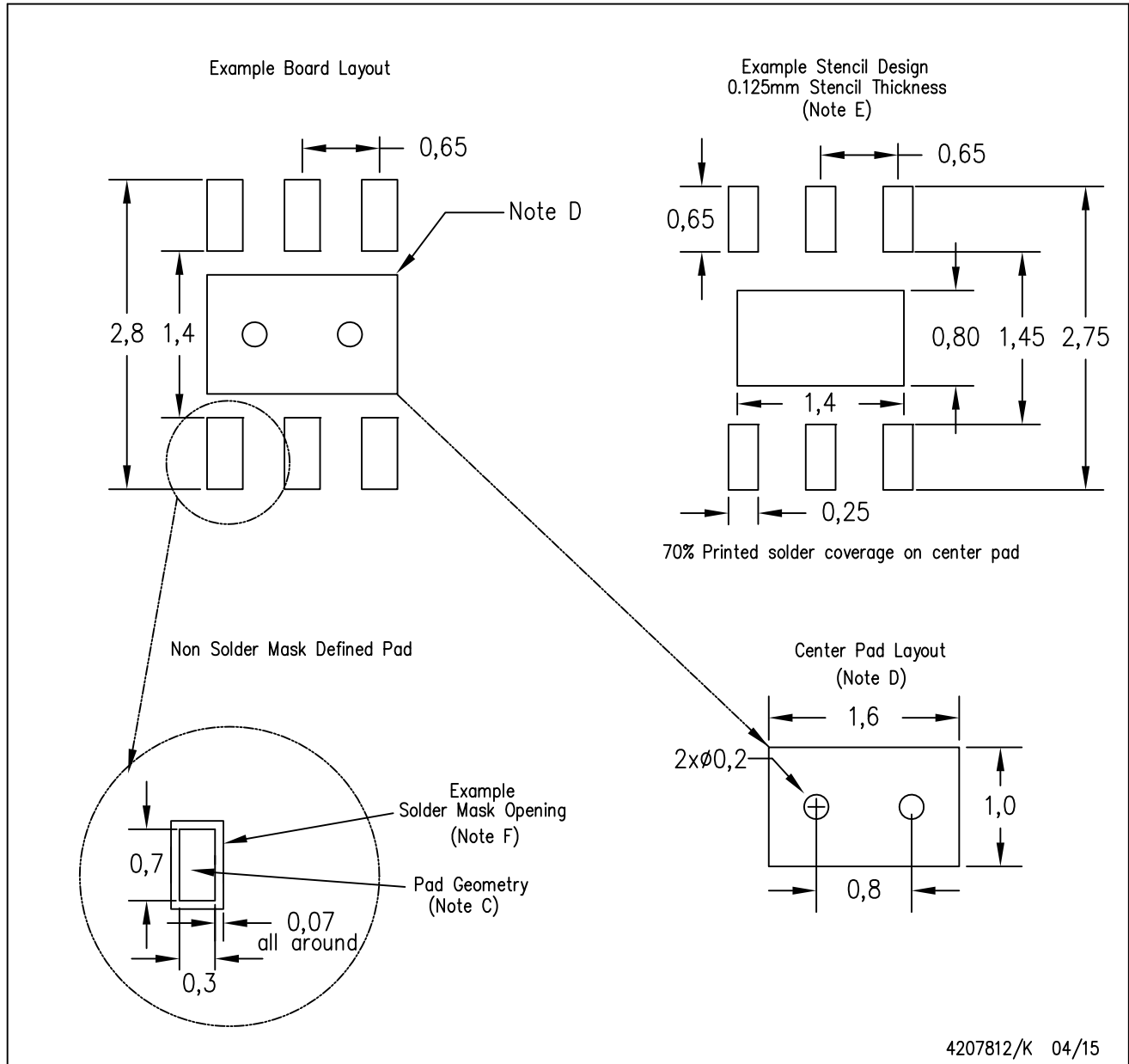
Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated