

## TPS65980 Thunderbolt™ Bus Power Buck/Boost

### 1 Features

- Powered From Thunderbolt™ Bus
- 2.5-V to 15.75-V Input
- 3.3-V Outputs
- Cable Power Out Current Limit
- Thermal Shutdown

### 2 Applications

- Thunderbolt™/Thunderbolt™ 2 Systems
- Bus Powered Systems
- Power Management Systems

### 3 Description

The TPS65980 DC/DC switching regulator that receives power from a Thunderbolt™ or Thunderbolt™ 2 power bus ranging from 2.5-V to 15.75-V and generates three separate 3.3-V supply outputs.

The TBT\_OUT supply provides power to the local peripheral Thunderbolt™ controller and support circuitry. The CBL\_OUT supply provides power back to the Thunderbolt™ cable and has adjustable current limit. The DEV\_OUT supply provides power to all other circuitry in the device to perform its designed function.

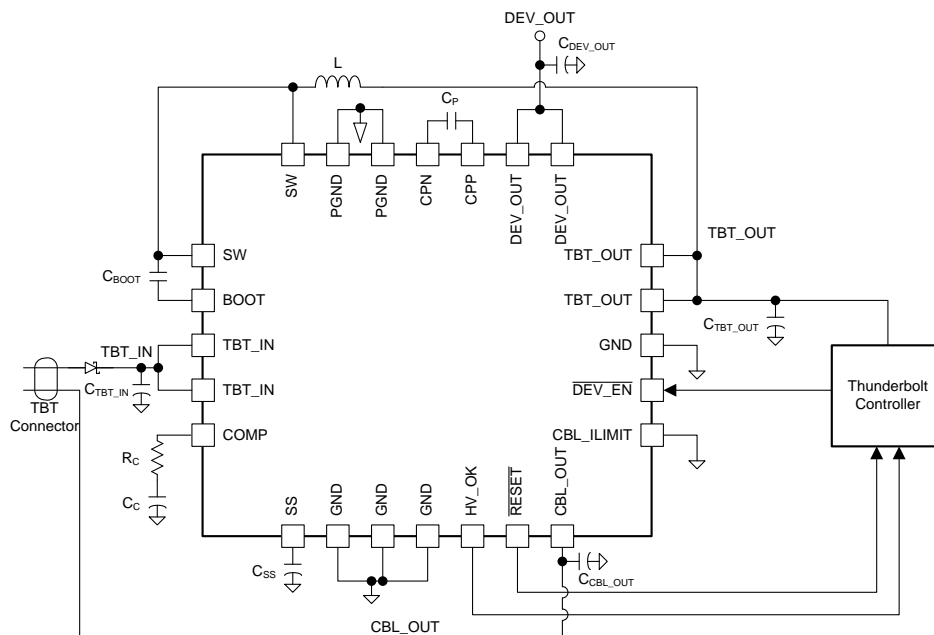
The TPS65980 is available in a 24-pin 5mm x 4mm x 0.9mm VQFN package.

#### Device Information<sup>(1)</sup>

DEVICE NAME	PACKAGE	BODY SIZE
TPS65980	VQFN (24)	5mm x 4mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### 4 Simplified Schematic



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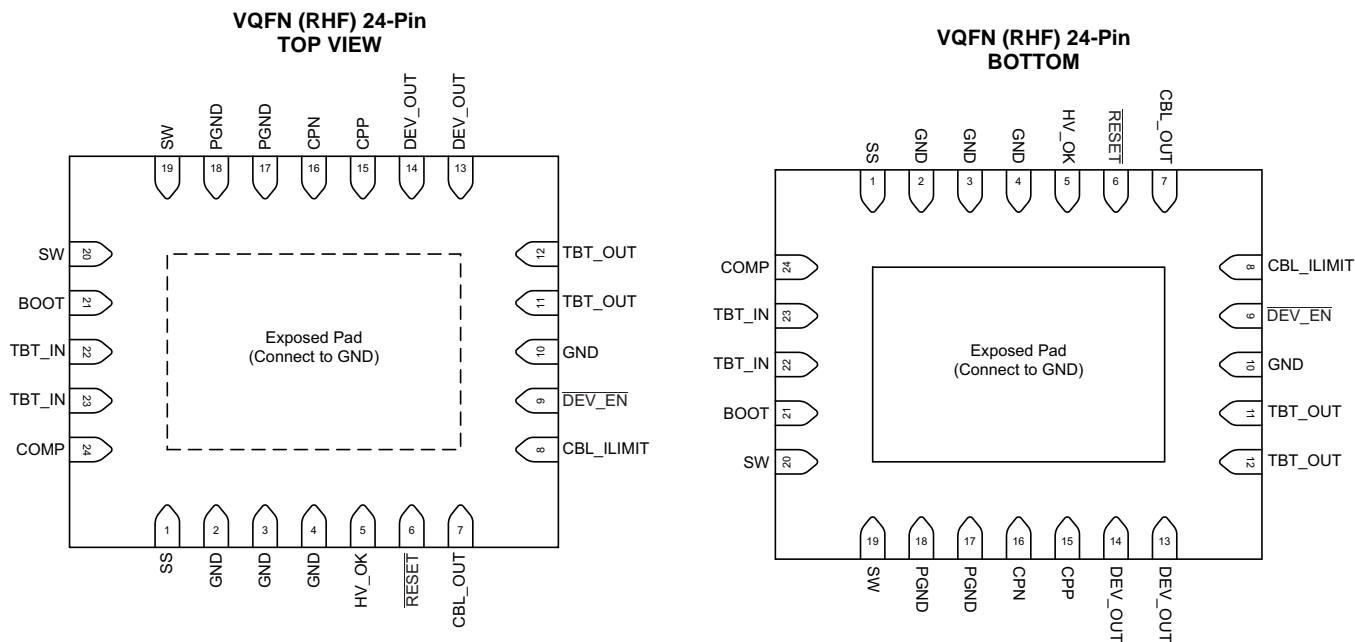
## 5 Revision History

### Changes from Original (April 2014) to Revision A

**Page**

• Revised document to full version. ....	<b>1</b>
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## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SS	ANALOG	Soft Start Capacitance. This pin sets the soft start ramp rate when the TBT_IN voltage ramps from 0V to high voltage.
2, 3, 4	GND	GND	Device Ground
5	HV_OK	OUTPUT	High Voltage Present Indicator. This pin indicates that a high voltage is present on TBT_IN. The output asserts high when the TBT_IN pin is above the V <sub>HVT</sub> voltage and the $\overline{\text{RESET}}$ output is asserting high.
6	$\overline{\text{RESET}}$	OUTPUT	Reset output indicator. This pin asserts low when TBT_OUT is in under-voltage.
7	CBL_OUT	PWROUT	Current Limited Power Output to Thunderbolt™ Cable. This pin supplies power to the Thunderbolt™ cable. The current limit of this pin is set by the CBL_ILIMIT pin.
8	CBL_ILIMIT	INPUT	Current Limit Set. Logic input that sets the current limit state on the CBL_OUT pin. Tie pin to TBT_OUT for a logic high input.
9	$\overline{\text{DEV\_EN}}$	INPUT	Device Enable Input. When input pin is high, DEV_OUT is high impedance. When input pin low, DEV_OUT is connected to TBT_OUT.
10	GND	ANALOG	Device Ground
11, 12	TBT_OUT	PWROUT	Power Output to Thunderbolt™ circuitry. This pin supplies power to the Thunderbolt™ controller.
13, 14	DEV_OUT	PWROUT	Power Output to peripheral device. This pin supplies power to circuitry not associated with the Thunderbolt™ controller or the Thunderbolt™ cable. It is intended to supply power to the peripheral device main function.
15	CPP	ANALOG	Charge Pump Capacitance Positive Output
16	CPN	ANALOG	Charge Pump Capacitance Negative Output
17, 18	PGND	GND	Buck Controller Power Ground
19, 20	SW	ANALOG	Buck Controller Switch Output
21	BOOT	ANALOG	Buck Controller Bootstrap
22, 23	TBT_IN	PWRIN	Power Input from Thunderbolt™ Cable. This pin is the power supply to the device.
24	COMP	ANALOG	Buck Converter Compensation. This pin provides compensation to the buck converter feedback loop.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage range <sup>(2)</sup>	TBT_IN	-0.3	18	V
	DEV_EN	-0.3	3.6	
	BOOT	-0.3	25	
	BOOT (10 ns transient)	-0.3	27	
	BOOT (vs SW)	-0.3	7	
	SW	-0.6	18	
	SW (10 ns transient)	-2	20	
	COMP	-0.3	3.6	
	SS	-0.3	3.6	
	CBL_ILIMIT	-0.3	3.6	
	CPP	-0.3	7.2	
CPN	-0.3	3.6		
Output voltage range <sup>(2)</sup>	TBT_OUT, CBL_OUT, DEV_OUT	-0.3	3.6	V
	RESET, HV_OK	-0.3	3.6	
V <sub>diff</sub>	Voltage from GND to Thermal Pad	-0.2	0.2	V
	Voltage from PGND to GND	-0.2	0.2	V
T <sub>A</sub>	Operating ambient temperature	-40	85	°C
T <sub>J</sub>	Operating junction temperature	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

### 7.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-55	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT	
TBT_IN	Supply input voltage range	2.5	15.75		
V <sub>I</sub>	Input voltage range	DEV_EN	-0.1	3.6	V
		BOOT	-0.1	25	
		SW	-0.6	16.5	
		COMP	-0.1	3.6	
		SS	-0.1	3.6	
		CBL_ILIMIT	-0.1	3.6	
		CPP	-0.1	7.2	
		CPN	-0.1	3.6	
V <sub>O</sub>	Output voltage range	TBT_OUT, CBL_OUT, DEV_OUT	-0.1	3.6	V
		RESET, HV_OK	-0.1	3.6	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	
T <sub>J</sub>	Operating junction temperature	-40	125	°C	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65980	UNIT
		RHF	
		24 PIN	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	30.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	26.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	8.2	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	8.2	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	1.5	

 (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

Unless otherwise noted all specifications applies over the  $V_{TBT\_IN}$  range and operating ambient temperature of  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $C_{TBT\_IN} = 22 \mu\text{F}$ ,  $C_{TBT\_OUT} = 10 \mu\text{F}$ ,  $C_{CBL\_OUT} = 1 \mu\text{F}$ ,  $CSS = 10 \text{ nF}$ , and 33 V/ $\mu\text{s}$  logic input transitions. Typical values are for  $V_{TBT\_IN} = 12 \text{ V}$  and  $T_A = 25^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>						
$V_{TBT\_IN}$	TBT_IN Input voltage range		2.5	12	15.75	V
$V_{REF\_RSTN}$	TBT_OUT to $\overline{\text{RESET}}$ clear high	TBT_OUT rising	3	3.1	3.2	V
	TBT_OUT to $\overline{\text{RESET}}$ assert low	TBT_OUT falling	2.5	2.6	2.7	
$V_{HVTR}$	TBT_IN to HV_OK assert	TBT_IN rising	4.36	4.5	4.64	V
$V_{HVTHYST}$	TBT_IN to HV_OK clear	TBT_IN Falling hysteresis		100		mV
$SR_{02L}$	TBT_IN Input slew rate	TBT_IN transition from 0 V to 3.3 V	0.1		30	kV/s
$SR_{L2H}$	TBT_IN Input slew rate	TBT_IN transition from 3.3 V to 15 V	0.1		30	kV/s
$I_{RAMP}$	Combined output di/dt <sup>(1)</sup>				5	kA/s
Efficiency	Buck converter efficiency	$I_{LOADTOTAL} = 3 \text{ A}$ , $V_{TBT\_IN} = 12 \text{ V}$		87%		
	Charge pump efficiency	$V_{TBT\_IN} = 3.3 \text{ V}$ , $I_{LOADTOTAL} = 25 \text{ mA}$		47%		
<b>POWER OUTPUT PINS (LOW VOLTAGE INPUT)<sup>(2)</sup></b>						
$V_{TBT\_IN}$	TBT_IN Input voltage range		2.5	3.3	3.4	V
$V_{TBT\_OUT}$	TBT_OUT Output voltage range <sup>(3)</sup>		3.135	3.25	3.4	V
$I_{TBT\_OUT}$	TBT_OUT Load current <sup>(4)(5)</sup>	$\overline{\text{RESET}}$ high	5		50	mA
		$\overline{\text{RESET}}$ low			100	$\mu\text{A}$
<b>POWER OUTPUT PINS (HIGH VOLTAGE INPUT)<sup>(6)</sup></b>						
$V_{TBT\_IN}$	TBT_IN Input voltage range		10	12	15.75	V
$V_{TBT\_OUT}$	TBT_OUT Output voltage range <sup>(3)</sup>	$I_{LOADTOTAL} = 1 \text{ A to } 3.5 \text{ A}$	3.221	3.27	3.319	V
		$I_{LOADTOTAL} = 0.235 \text{ A to } 3.5 \text{ A}$	3.221	3.27	3.42	
$I_{TBT\_OUT}$	TBT_OUT Load current <sup>(4)</sup>		235		1000	mA
$V_{CBL\_OUT}$	CBL_OUT Output voltage range <sup>(3)</sup>	$ILIMIT = 0$ , $I_{CBL\_OUT} = 0 \text{ to } 720 \text{ mA}$	3.171	3.27	3.319	V
		$ILIMIT = 1$ , $I_{CBL\_OUT} = 0 \text{ to } 1.44 \text{ A}$	3.12	3.27	3.319	
$V_{DEV\_OUT}$	DEV_OUT Output Voltage Range	$I_{DEV\_OUT} = 0 \text{ to } 2500 \text{ mA}$	3	3.27	3.319	V
<b>POWER OUTPUT PINS (HIGH VOLTAGE INPUT DURING SYSTEM SLEEP)</b>						
$V_{TBT\_IN}$	TBT_IN Input voltage range		5.2	12	15.75	V
$V_{TBT\_OUT}$	TBT_OUT DC Output voltage range	$I_{LOADTOTAL} = 1 \text{ A to } 3.5 \text{ A}$	3.221	3.27	3.319	V
		$I_{LOADTOTAL} = 0.235 \text{ A to } 3.5 \text{ A}$	3.221	3.27	3.42	
$I_{TBT\_OUT}$	TBT_OUT Load current		5		31	mA
$V_{CBL\_OUT}$	CBL_OUT Output voltage range <sup>(3)</sup>	$I_{CBL\_OUT} = 0 \text{ to } 235 \text{ mA}$	3.171	3.27	3.319	V
$V_{DEV\_OUT}$	DEV_OUT Output voltage range	$I_{DEV\_OUT} = 0 \text{ to } 700 \text{ mA}$	3	3.3	3.319	V
<b>CABLE OUTPUT (HIGH VOLTAGE INPUT &amp; HIGH VOLTAGE INPUT DURING SLEEP)</b>						
$V_{CBL\_OUT\_MON}$	CBL_OUT Ramp-up monotonicity <sup>(7)</sup>	CBL_OUT ramp from off to on			0	mV
$V_{CBL\_OUT\_RIP}$	CBL_OUT Voltage ripple	After settling All output combined Load > 1 mA			2	%P-P
		All output combined Load < 1 mA			40	mV <sub>P=P</sub>
$I_{LIM\_CBL\_OUT}$	CBL_OUT Current limit	$ILIMIT = 0$	0.8	1.1	1.4	A
		$ILIMIT = 1$	1.6	2.2	2.8	
$t_{LIM\_CBL\_OUT}$	Short circuit response time	$RCBL\_OUT = 0.5 \Omega \text{ to GND}$ , $ILIMIT = 0$			500	$\mu\text{s}$
		$RCBL\_OUT = 0.01 \Omega \text{ to GND}$ , $ILIMIT = 0$			8	

- (1) The three voltage outputs (TBT\_OUT, CBL\_OUT, DEV\_OUT) all pull current from a single node. Therefore, the total combined current cannot exceed the maximum di/dt.
- (2) CBL\_OUT and DEV\_OUT are open (high impedance) for this input voltage range.
- (3) During light load conditions, the average output voltage may reach 3.5 V with peaks not exceeding 3.42 V.
- (4) TBT\_OUT load current flows from the TBT\_OUT pin when the device is in charge pump mode and pulls the buck converter inductor when the device is in buck mode.
- (5) TBT\_OUT load current will not go higher than 50mA until after the device asserts HV\_OK.
- (6) The maximum current supplied by the TPS65980 to all outputs is limited to 3.5 A. Max power depends on the Thunderbolt™ system and how much power is supplied to the input.
- (7) A monotonicity of 0 mV means that the output does not have a negative going ramp at anytime during its power up ramp. A ripple of up to 62 mV from the DC/DC will occur.

## Electrical Characteristics (continued)

Unless otherwise noted all specifications applies over the  $V_{TBT\_IN}$  range and operating ambient temperature of  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $C_{TBT\_IN} = 22 \mu\text{F}$ ,  $C_{TBT\_OUT} = 10 \mu\text{F}$ ,  $C_{CBL\_OUT} = 1 \mu\text{F}$ ,  $CSS = 10 \text{ nF}$ , and 33 V/ $\mu\text{s}$  logic input transitions. Typical values are for  $V_{TBT\_IN} = 12 \text{ V}$  and  $T_A = 25^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DEV_EN AND ILIMIT INPUT LOGIC</b>						
$V_{IH}$	High-level input voltage		2.6			V
$V_{IL}$	Low-level input voltage				0.6	V
$I_{IN}$	Input leakage to GND	$V_{DEV\_EN} = 3.3\text{V}$			1	mA
<b>RESET AND HV_OK OUTPUT LOGIC</b>						
$V_{OH}$	High-level output voltage	$I_L = -1.5 \text{ mA}$ , Referenced to $V_{TBT\_OUT}$	-250		0	mV
$V_{OL}$	Low-level output voltage	$I_L = 1.5 \text{ mA}$	0		250	mV
<b>SOFT START<sup>(8)</sup></b>						
$I_{INRUSH}$	Inrush current di/dt				250	kA/s
<b>THERMAL SHUTDOWN</b>						
$T_{SD}$	Shutdown temperature		120	135	150	$^{\circ}\text{C}$
$T_{SDHYST}$	Shutdown hysteresis			10		$^{\circ}\text{C}$

(8) The charge pump will limit the normal ramp of current. Soft start will control the inrush current when the input ramps from 0 V to high voltage (not a normal operating condition). See recommended components section for required soft-start cap.

## 7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
$t_{IN2OR}$	TBT_IN to TBT_OUT On Time	$V_{TBT\_IN} \geq 0.9 \times V_{TBT\_IN(min)}$ to $V_{TBT\_OUT} \geq 0.99 \times V_{TBT\_OUT(min)}$ $R_{TBT\_OUT} = 100 \Omega$			20	ms
$t_{IN2OF}$	TBT_IN to TBT_OUT Off Time	$V_{TBT\_IN} \leq 0.9 \times V_{TBT\_IN(min)}$ to $V_{TBT\_OUT} \leq 0.1 \times V_{TBT\_OUT(min)}$ $R_{TBT\_OUT} = 100 \Omega$		2.4	4	ms
$t_{OUT2RR}$	TBT_OUT to RESETZ High time	$V_{TBT\_OUT} \geq V_{REF\_RSTN(max)}$ rising to $V_{RESET} = 0.9 \times V_{OH}$ , $C_{RESETN} = 100 \text{ pF}$			20	$\mu\text{s}$
$t_{IN2RF}$	TBT_IN to RESETZ Low time	$V_{TBT\_IN} \leq 0.9 \times V_{TBT\_IN(min)}$ to $V_{RESET} = 0.1 \times V_{OH}$ , $C_{RESETN} = 100 \text{ pF}$			20	ms
$t_{HV2OKR}$	TBT_IN Rise to HV_OK	$V_{TBT\_IN} \geq V_{HVTR}$ to $V_{HV\_OK} = 0.9 \times V_{OH}$ $C_{HV\_OK} = 100 \text{ pF}$			10	$\mu\text{s}$
$t_{HV2OKF}$	TBT_IN Fall to HV_OK	$V_{TBT\_IN} \leq V_{HVTR} - V_{HVTHYST}$ to $V_{HV\_OK} = 0.1 \times V_{OH}$ , $C_{HV\_OK} = 100 \text{ pF}$			10	$\mu\text{s}$
$t_{HV2CR}^{(1)(2)}$	HV_OK to CBL_OUT On time	$V_{HV\_OK} \geq 1.65 \text{ V}$ to $V_{CBL\_OUT} = 2.95 \text{ V}$ $R_{CBL\_OUT} = 100 \Omega$ , $C_{HV\_OK} = 100 \text{ pF}$	0.1		10	ms
$t_{HV2CF}$	HV_OK to CBL_OUT Off time	$V_{HV\_OK} \leq 1.65 \text{ V}$ to $V_{CBL\_OUT} = 2.95 \text{ V}$ $R_{CBL\_OUT} = 100 \Omega$ , $C_{HV\_OK} = 100 \text{ pF}$			40	$\mu\text{s}$
$t_{RCBL}$	CABLE_OUT Ramp time	$V_{CBL\_OUT}$ ramp 10% to 90% $C_{CBL\_OUT} = 0$ to $52 \mu\text{F}$	0.1		10	ms
$t_{DEVEN}$	$\overline{DEV\_EN}$ to DEV_OUT On time	$V_{DEV\_EN} \leq 1.65 \text{ V}$ to $V_{DEV\_OUT} = 2.7 \text{ V}$ $R_{DEV\_OUT} = 100 \Omega$	0.1		10	ms
$t_{DEVDIS}$	$\overline{DEV\_EN}$ to DEV_OUT Off time	$V_{DEV\_EN} \geq 1.65 \text{ V}$ to $V_{DEV\_OUT} = 2.7 \text{ V}$ $R_{DEV\_OUT} = 100 \Omega$			50	ms
$t_{HV2DEVEN}$	Wait time from HV_OK High before $\overline{DEV\_EN}$ can be asserted low <sup>(2)</sup>	$V_{HV\_OK} \geq 1.65 \text{ V}$ to $V_{DEV\_EN} \leq 1.65 \text{ V}$ $C_{HV\_OK} = 100 \text{ pF}$	2			ms

(1) TBT\_IN must transition from 3.3 V to high voltage, not from 0 V to high voltage

(2) During the transition from low voltage input to high voltage input, the total load of all outputs combined can not exceed 85 mA until 2 ms after HV\_OK asserts high.

## 7.7 Timing Diagrams

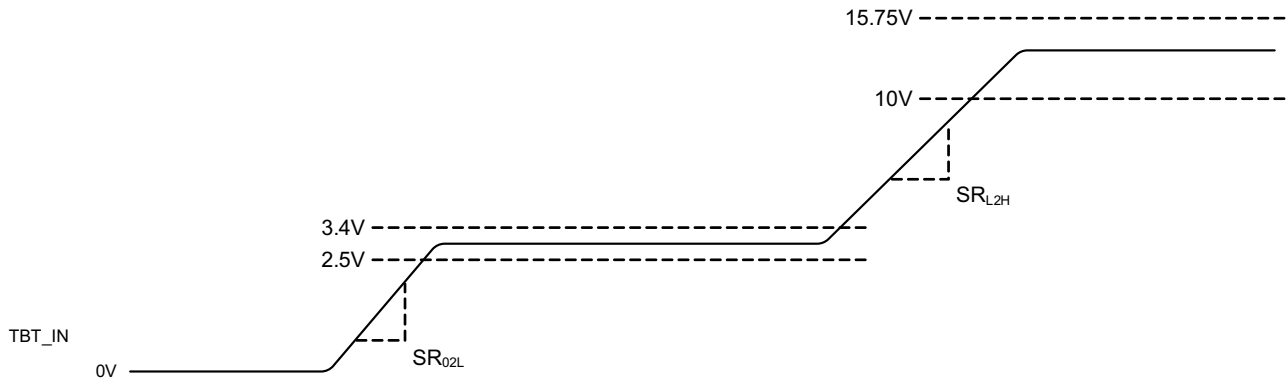


Figure 1. TBT\_IN Slew Rates

The TPS65980 has two normal operating regions. The first region is when  $2.5\text{ V} \leq V_{\text{TBT\_IN}} \leq 3.4\text{ V}$ . This is the normal power-up state and is termed the low-voltage state. When the input transitions to this range, the input slew rate must meet the  $\text{SR}_{02\text{L}}$  limits. In this voltage range, the TPS65980 operates with a charge pump to generate the nominally 3.3 V output. When the input voltage moves to the higher end of this range, the buck converter takes over to produce the 3.3 V. In normal operation, the TPS65980 input voltage will transition from the low-voltage range to a high-voltage range where  $10\text{ V} \leq V_{\text{TBT\_IN}} \leq 15.75\text{ V}$ . This is the high-voltage state and is the state where the TPS65980 will operate most of the time. In this state, the device operates as a buck converter providing a nominally 3.3 V output. Figure 1 shows the input voltage transitions and states.

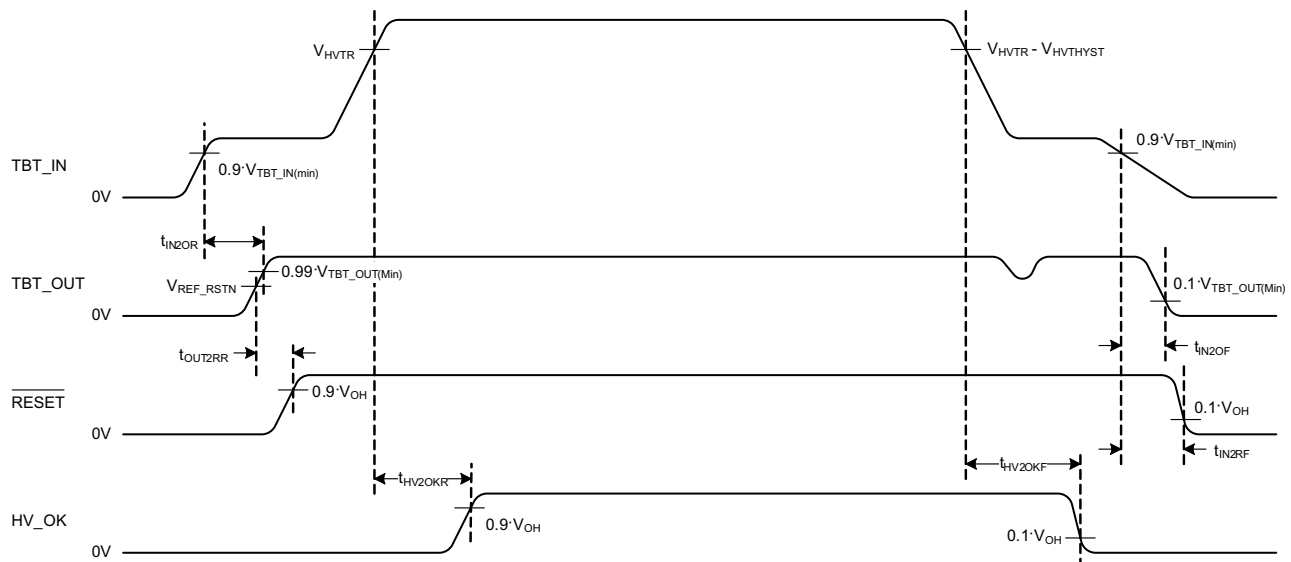
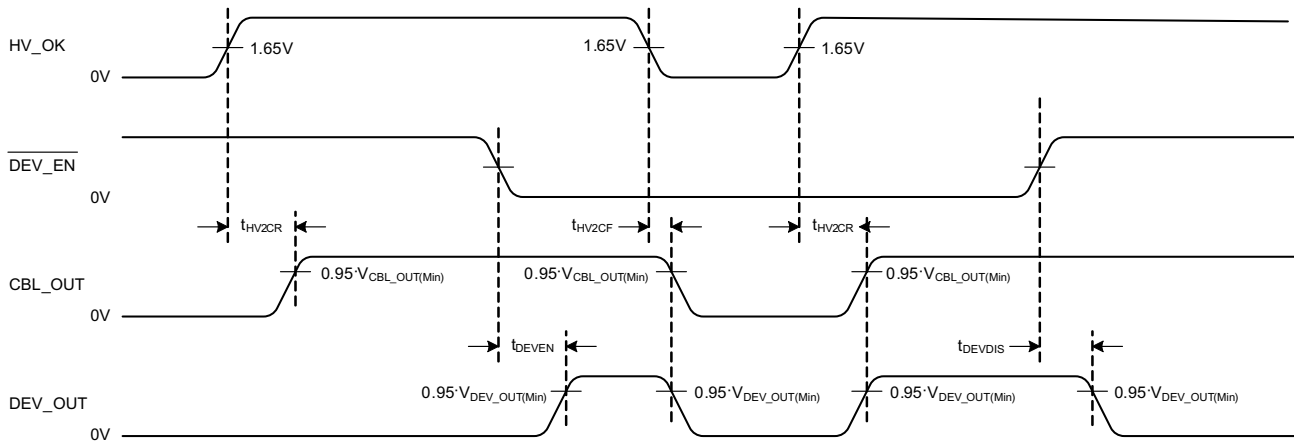


Figure 2. Timing Diagram

Figure 2 shows normal operating timing diagram for the TBT\_OUT output voltage and the  $\overline{\text{RESET}}$  and HV\_OK output indicator signals. When TBT\_IN transitions to the low-voltage range, TBT\_OUT will power up a short time later. Once TBT\_OUT reaches the normal output range,  $\overline{\text{RESET}}$  will transition high. However, timing for  $\overline{\text{RESET}}$  is measured from the input TBT\_IN transitioning high. When TBT\_IN transitions from the low-voltage input range to the high-voltage input range, HV\_OK will transition high.  $\overline{\text{RESET}}$  is an active-high output indicating that the TBT\_OUT voltage is valid and. HV\_OK is an active-high output indicating that the TBT\_IN voltage is in the high-voltage range. When in the high-voltage state, the TPS65980 can provide much higher output current than when in the low-voltage state.

### Timing Diagrams (continued)

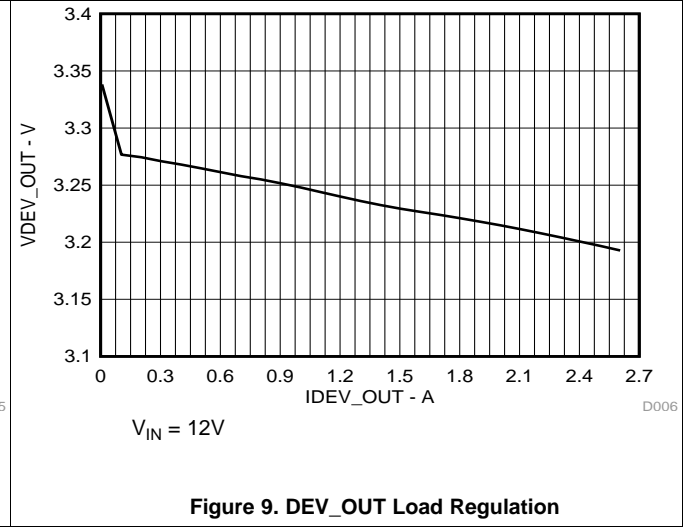
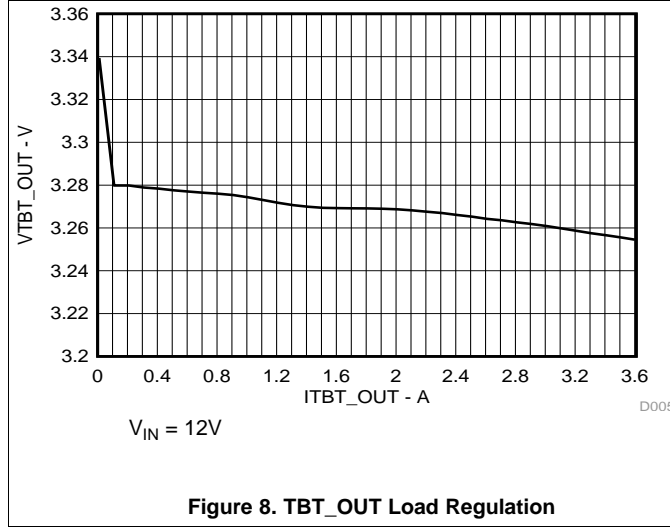
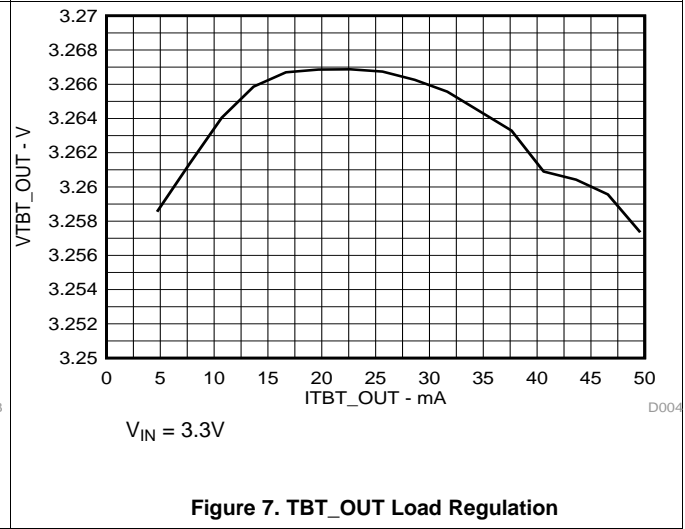
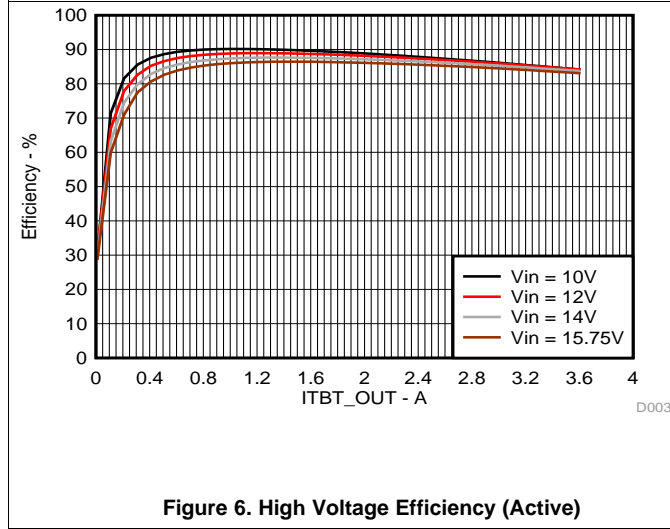
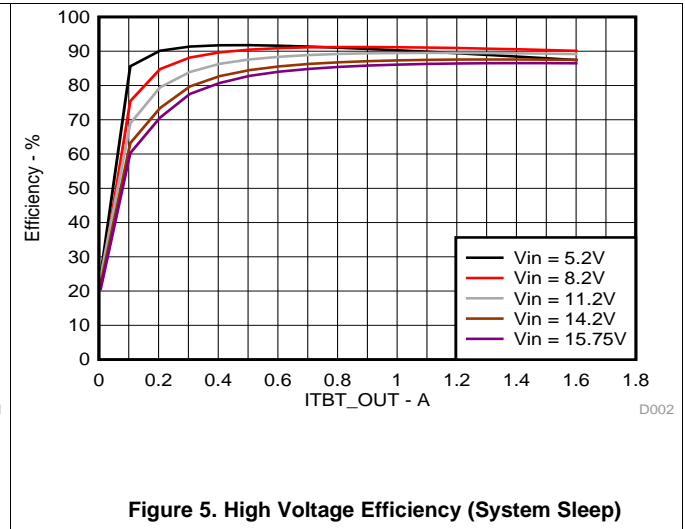
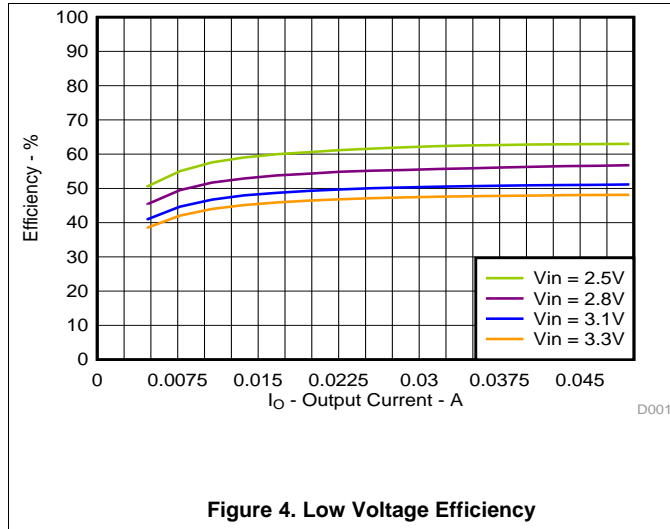
When the TBT\_IN input transitions from high-voltage to low-voltage, HV\_OK will de-assert to a logic low. When the TBT\_IN input voltage falls below the minimum operating voltage, the RESET output will de-assert low.



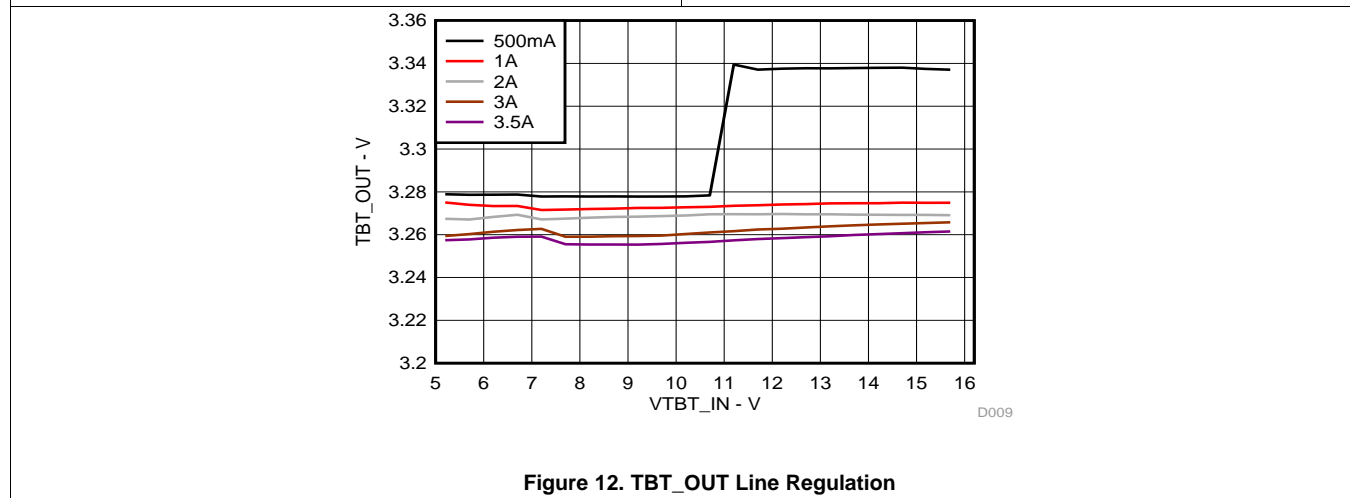
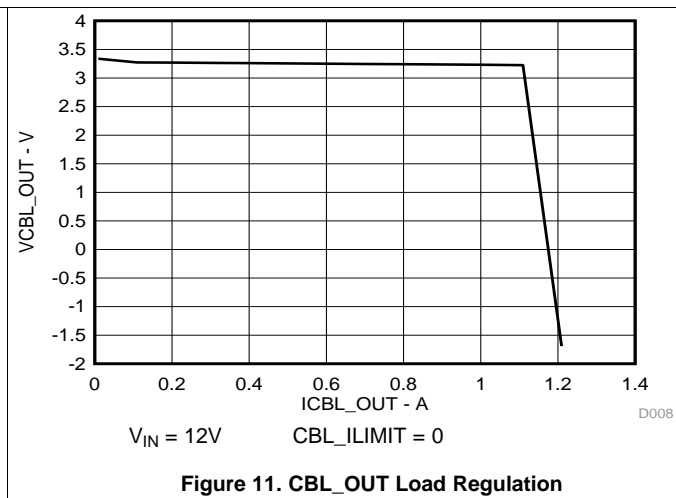
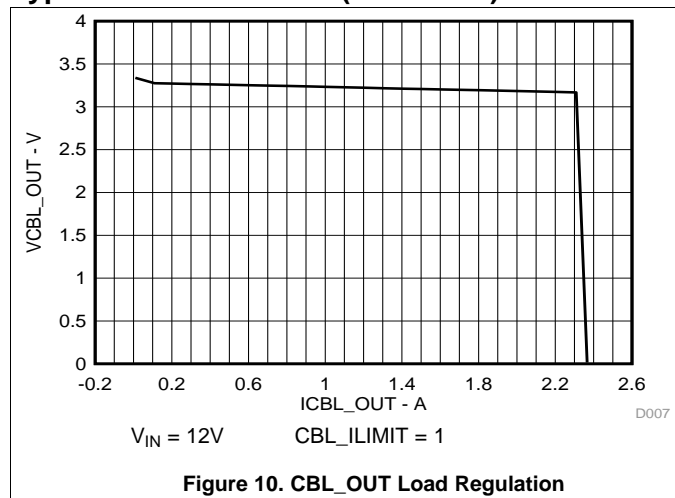
**Figure 3. Timing Diagram**

Figure 3 shows the CBL\_OUT and DEV\_OUT outputs and timing based on the HV\_OK signal and the DEV\_ENZ input. The CBL\_OUT output will be connected to TBT\_OUT and supplying 3.3V when HV\_OK is asserting high. The DEV\_OUT output will be connected to TBT\_OUT and supplying 3.3 V when HV\_OK is asserting high and the DEV\_ENZ input is low.

## 7.8 Typical Characteristics



Typical Characteristics (continued)



## 8 Detailed Description

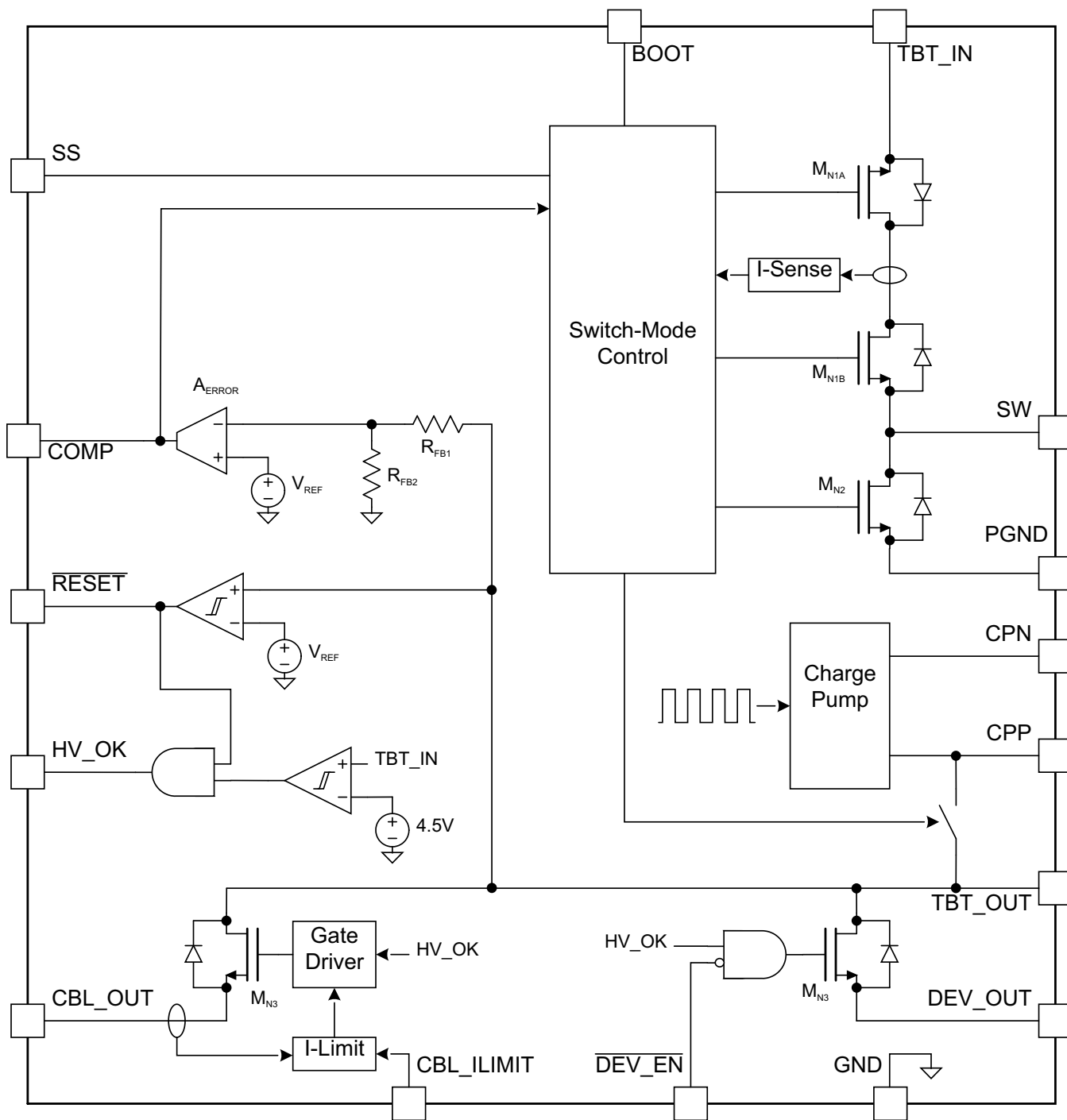
### 8.1 Overview

The TPS65980 is a switching regulator designed for Thunderbolt™ and Thunderbolt™ 2 bus-powered systems. The TPS65980 receives power from a Thunderbolt™ host in the range of 2.5 V to 15.75 V and produces three separate 3.3 V outputs. TBT\_OUT is the main output from the regulator. This output is generated from a switched-cap charge pump when the input is in the low-voltage range. The output is generated from a switching buck converter when the input voltage is in the high-voltage range. The TBT\_OUT output powers the local Thunderbolt™ controller and any additional Thunderbolt™ circuitry. Once in the input has settled in the high-voltage range, the other two outputs can be powered from the TBT\_OUT output. When the TBT\_OUT is supplying 3.3 V, the  $\overline{\text{RESET}}$  output asserts high. When the TBT\_OUT voltage is below the valid output range,  $\overline{\text{RESET}}$  asserts low. When TBT\_IN is in the high-voltage input range and  $\overline{\text{RESET}}$  is asserting high (valid output), HV\_OK will assert high indicating that high-voltage has been received.

The CBL\_OUT output supplies power back to the Thunderbolt™ cable for powering the active cable circuitry. This output is connected to the TBT\_OUT output with a FET switch and is current limited.

The CBL\_ILIMIT logic input pin sets the current limit level. The DEV\_OUT output provides power to all other circuitry in the system. This output is not current limited and is enabled/disabled by the  $\overline{\text{DEV\_EN}}$  logic input.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 2.5-V to 15.75-V Input

The TPS65980 is powered from a Thunderbolt™ Bus. This is typically an input to a port from Thunderbolt™ cable. This input will start at 3.3 V ( $2.5\text{ V} \leq V_{\text{TBT\_IN}} \leq 3.4\text{ V}$ ) until a link is established between a host and the peripheral device containing the TPS65980. Once the link is established, the voltage at the input can transition to a higher operating voltage ( $10\text{ V} \leq V_{\text{TBT\_IN}} \leq 15.75\text{ V}$ ).

### 8.3.2 3.3-V Outputs

The TPS65980 has three separate 3.3 V outputs. One output, TBT\_OUT, is the output from the buck/boost and the other outputs, CBL\_OUT and DEV\_OUT, are outputs that through load switches from TBT\_OUT.

The TBT\_OUT supply provides power to the local peripheral Thunderbolt™ controller and support circuitry. The CBL\_OUT supply provides power back to the Thunderbolt™ cable and has adjustable current limit. The DEV\_OUT supply provides power to all other circuitry in the device to perform its designed function.

### 8.3.3 Thermal Shutdown

The TPS65980 has a thermal shutdown feature preventing the device from over heating during current limiting situations. The thermal shutdown occurs at a 135°C junction temperature typically. A 10°C hysteresis occurs before the thermal shutdown is cleared.

### 8.3.4 Cable Power Out Current Limit

The CBL\_OUT output is current limited internally. The current limit has two values which are set by the CBL\_ILIMIT logic input. When CBL\_ILIMIT = 0, the current limit will be set to 1.1 A typically. When CBL\_ILIMIT = 1, the current limit will be set to 2.2 A typically.

## 8.4 Device Functional Modes

### 8.4.1 Operation with $2.5\text{ V} \leq V_{\text{TBT\_IN}} \leq 3.4\text{ V}$

The TPS65980 has two normal operating regions. The first region is when  $2.5\text{ V} \leq V_{\text{TBT\_IN}} \leq 3.4\text{ V}$ . This is the normal power-up state and is termed the low-voltage state. When the input transitions to this range, the input slew rate must meet the SR02L limits. In this voltage range, the TPS65980 operates with a charge pump to generate the nominally 3.3 V output. When the input voltage moves to the higher end of this range, the buck converter takes over to produce the 3.3 V.

### 8.4.2 Operation with $10\text{ V} \leq V_{\text{TBT\_IN}} \leq 15.75\text{ V}$

In normal operation, the TPS65980 input voltage will transition from the low-voltage range to a high-voltage range where  $10\text{ V} \leq V_{\text{TBT\_IN}} \leq 15.75\text{ V}$ . This is the high-voltage state and is the state where the TPS65980 will operate most of the time. In this state, the device operates as a buck converter providing a nominally 3.3 V output.

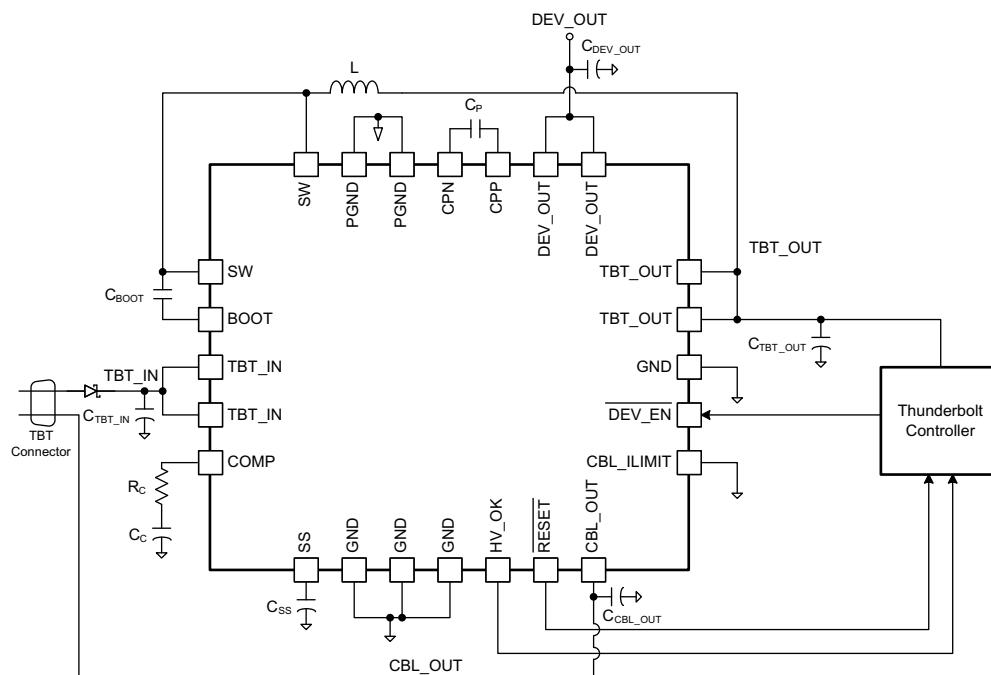
## 9 Application and Implementation

### 9.1 Application Information

The TPS65980 DC/DC switching regulator that receives power from a Thunderbolt™ or Thunderbolt™ 2 power bus ranging from 2.5 V to 15.75 V and generates three separate 3.3-V supply outputs.

### 9.2 Typical Application

#### 9.2.1 Single-Port Bus-Powered Thunderbolt™ Device



**Figure 13. Typical Application (Single-Port Bus-Powered Thunderbolt™ Device)**

#### 9.2.1.1 Design Requirements

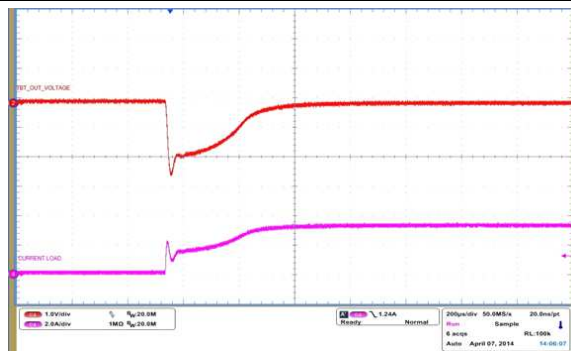
**Table 1. Recommended Component Values**

COMPONENT	DESCRIPTION	MIN	TYP	MAX	UNIT
C <sub>IN</sub>	TBT_IN Input Capacitance	17.6	22	52	μF
C <sub>BOOT</sub>	Converter Bootstrap Capacitance	8	10	12	nF
C <sub>CP</sub>	Charge Pump Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	μF
C <sub>SS</sub>	Soft Start Capacitance	8	10	12	nF
C <sub>TBT</sub>	TBT_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	16	20	24	μF
C <sub>CBL</sub>	CBL_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	μF
C <sub>DEV</sub>	DEV_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	μF
C <sub>C</sub>	Compensation Capacitance	8	10	12	nF
R <sub>C</sub>	Compensation Resistance	8	10	12	kΩ
L	Inductor SRR1280 (ESR ≤ 20 mΩ)	8	10	12	μH

#### 9.2.1.2 Detailed Design Procedure

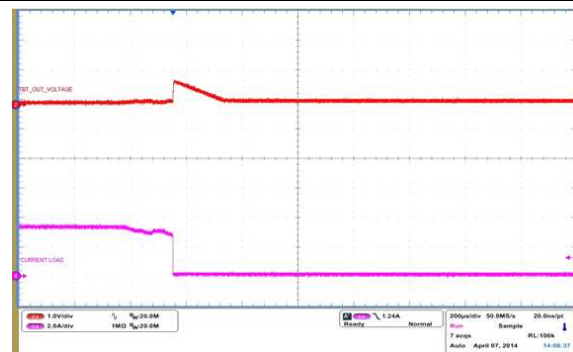
The TPS65980 should use the recommended component values in [Table 1](#). The device is designed to fit the needs of a Thunderbolt™ bus powered peripheral and the recommended component values are chosen to satisfy those conditions. The input capacitance C<sub>IN</sub> can be as high as 52 μF, but this maximum capacitance must include all capacitances seen at the input to the Thunderbolt™ port.

9.2.1.3 Application Performance Plots



$C_{TBT\_OUT} = 10 \mu F$        $V_{TBT\_IN} = 12 V$

Figure 14. TBT\_OUT Load Transient Response (0.5A to 3.5A Step)



$C_{TBT\_OUT} = 10 \mu F$        $V_{TBT\_IN} = 12 V$

Figure 15. TBT\_OUT Load Transient Response (3.5A to 0.5A Step)



Figure 16. 0V to 3.3V Power Up With 50mA Load



Figure 17. 3.3V to 0V Power Down With 50mA Load



Figure 18. 3.3V to 15.75V Vin Step With 50mA Load

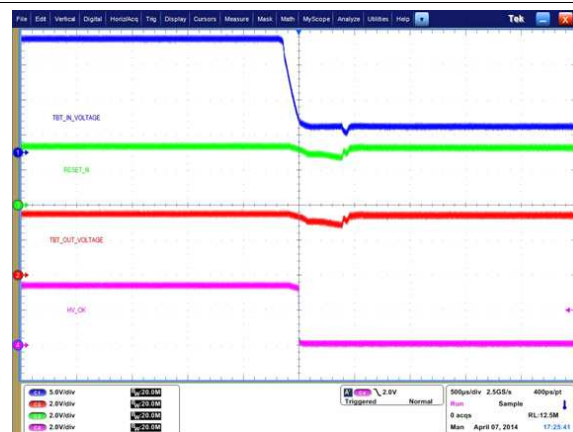
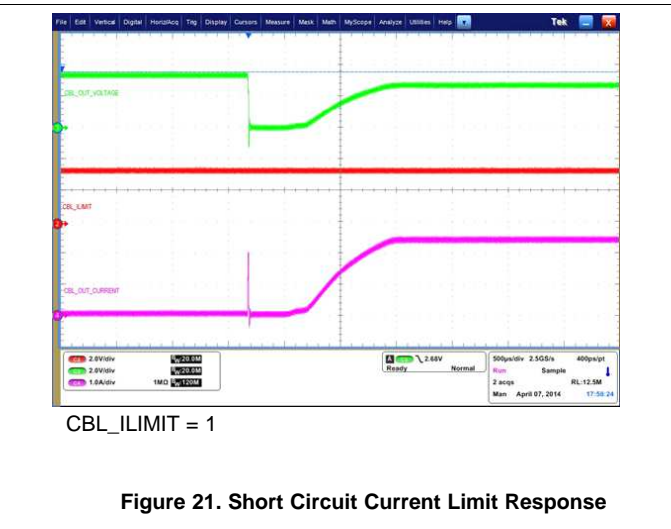
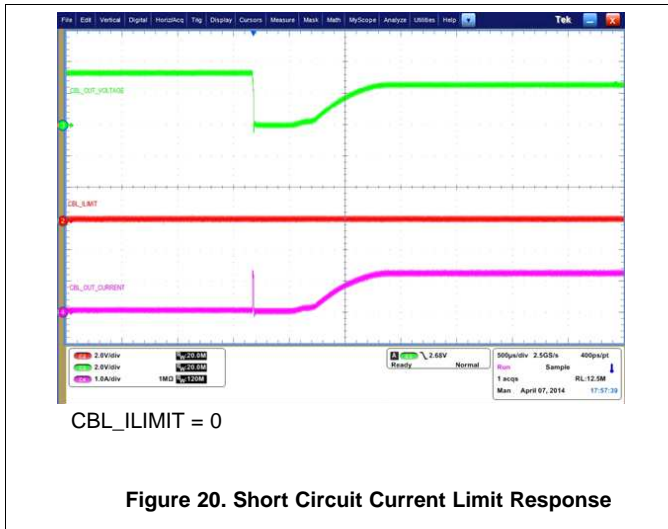
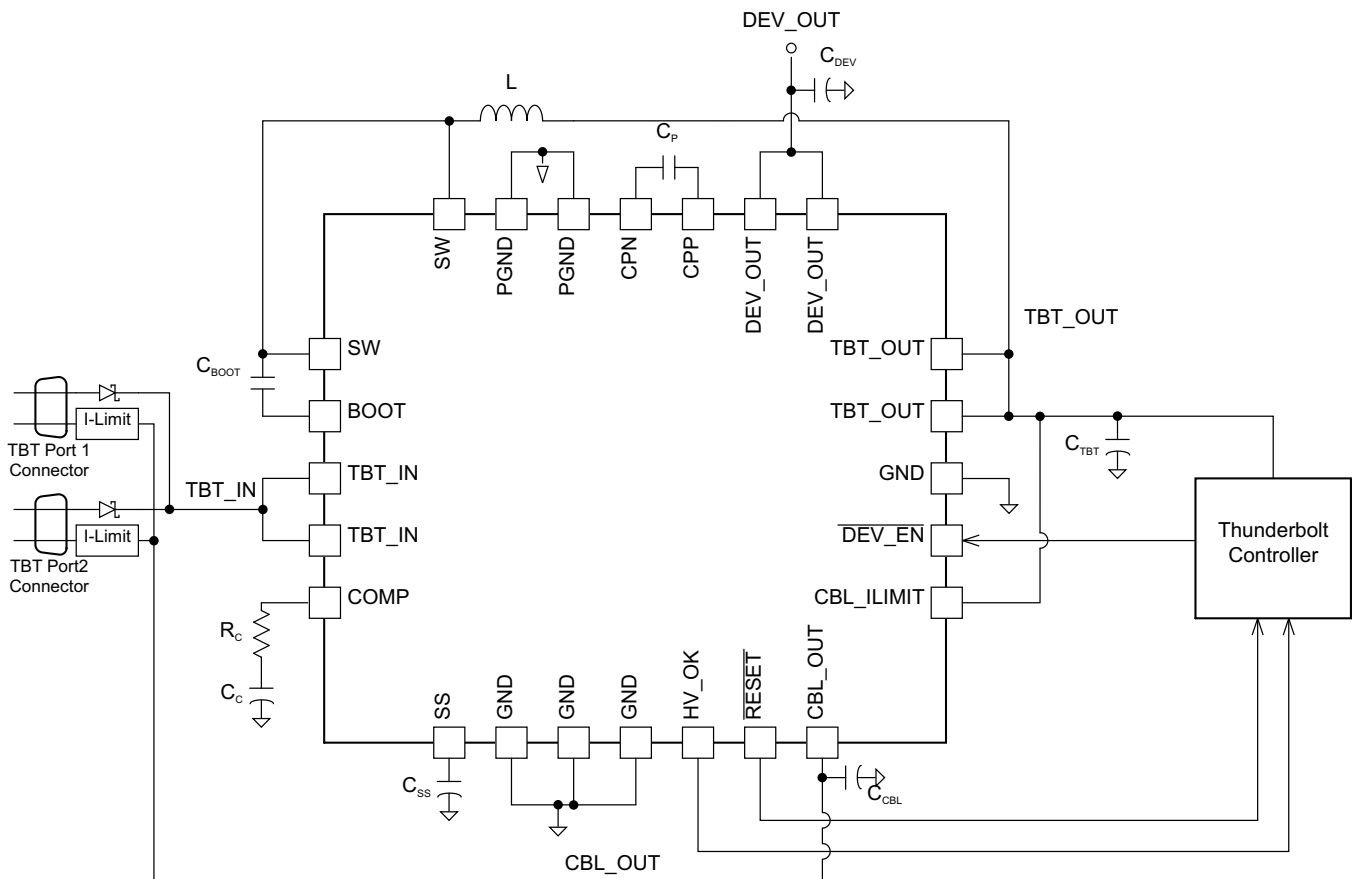


Figure 19. 15.75 to 3.3V Vin Step With 50mA Load



## 9.2.2 Dual-Port Bus-Powered Thunderbolt™ Device



**Figure 22. Typical Application (Dual-Port Bus-Powered Thunderbolt™ Device)**

### 9.2.2.1 Design Requirements

In a dual-port application, the TBT\_IN input voltage will be selected from either port. A simple diode-or function will produce TBT\_IN from the higher of the two inputs. The diode-or selection will allow the high-voltage supply to be at TBT\_IN.

In a dual port system, the TPS65980 must provide cable power to both ports. In this case, a second current limiting device (TPS22920) connected between TBT\_OUT and the port is recommended. The CBL\_OUT pin can also supply current to both ports. In this case, tying CBL\_ILIMIT to TBT\_OUT will double the amount of current that can be supplied before current limiting. When using this method, the voltage drop to the CBL\_OUT pin will increase and care must be taken that other systems resistance do not cause the cable voltage to drop below the allowed pin voltage specified in the Thunderbolt™ specification. To avoid issues with voltage drop in the system, it is recommended that the second port be powered from TBT\_OUT as shown in [Figure 22](#). This relieves the voltage drop due to extra current through the CBL\_OUT load switch.

**Table 2. Recommended Component Values**

COMPONENT	DESCRIPTION	MIN	TYP	MAX	UNIT
C <sub>IN</sub>	TBT_IN Input Capacitance	17.6	22	52	μF
C <sub>BOOT</sub>	Converter Bootstrap Capacitance	8	10	12	nF
C <sub>CP</sub>	Charge Pump Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	μF
C <sub>SS</sub>	Soft Start Capacitance	8	10	12	nF
C <sub>TBT</sub>	TBT_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	16	20	24	μF
C <sub>CBL</sub>	CBL_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	μF
C <sub>DEV</sub>	DEV_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	μF
C <sub>C</sub>	Compensation Capacitance	8	10	12	nF
R <sub>C</sub>	Compensation Resistance	8	10	12	kΩ
L	Inductor SRR1280 (ESR ≤ 20 mΩ)	8	10	12	μH

### 9.2.2.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#) in the [Single-Port Bus-Powered Thunderbolt™ Device](#) section.

### 9.2.2.3 Application Performance Plots

Refer to [Application Performance Plots](#) in the [Single-Port Bus-Powered Thunderbolt™ Device](#) section.

## 10 Power Supply Recommendations

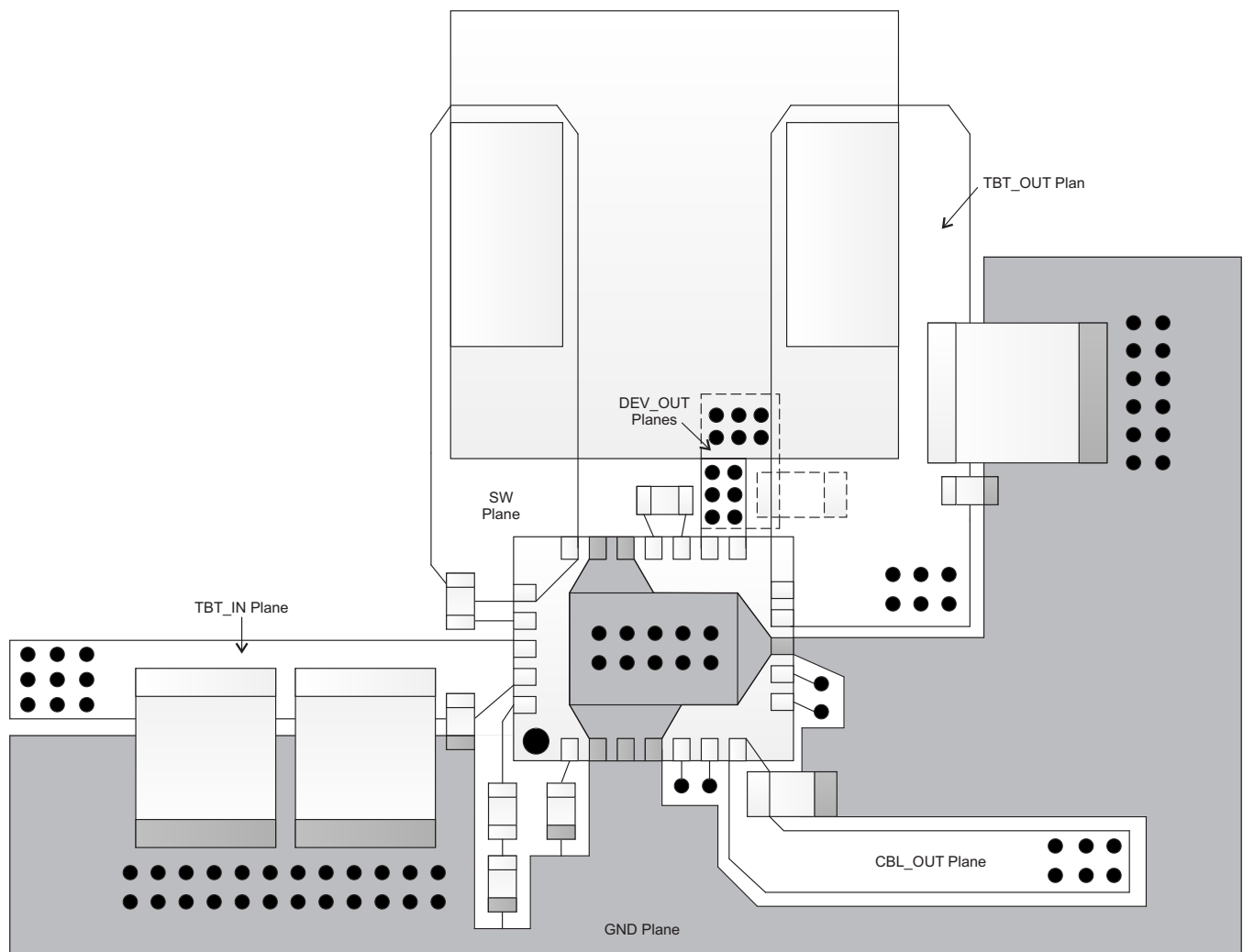
The TPS65980 is designed to operate from a Thunderbolt™ bus. The input will range from 2.5 V to 15.75 V. The input should be placed as near to the port connector as possible.

## 11 Layout

### 11.1 Layout Guidelines

Proper placement and routing will maximize the performance of the TPS65980. Follow [Figure 23](#) for optimized layout and routing (hashed planes indicate bottom layer).

### 11.2 Layout Example



**Figure 23. Top View Board Layout**

### Layout Example (continued)

For TBT\_IN, the input capacitors must be placed close to the device with an inductance less than 1nH from input capacitors to the TBT\_IN pins. Layout tools and calculators are available to approximate the inductance. The input capacitors must have their GND side area via stitched to the GND plane. The GND side of the input cap should also share the same polygon as the PGND/PowerPad on the top layer. PowerPad should be connected to the GND plane through multiple vias.

Inductor placement should be above the TPS65980, slightly to the left of the device. The SW pins to the inductor must be connected through a plane as shown in Figure 23. The TBT\_OUT pins also have to be connected to the other side of the inductor with a plane. This plane should be wide to overlap the output capacitors. The GND side of the output capacitors should be stitched to the GND plane.

The CBL\_OUT output capacitor should be placed close to the device on the top layer with an inductance less than 1 nH from the capacitor to the CBL\_OUT pin. The DEV\_OUT capacitor is best placed on the bottom side of the board with two planes (top and bottom) connect through a set of vias. The number of vias placed should be able to carry at least 3 A (DEV\_OUT = 2.5 A max) for margin and inductance path less than 1nH from DEV\_OUT pins to capacitor. When routing DEV\_OUT to an internal power plane, follow Figure 24 for via paths.

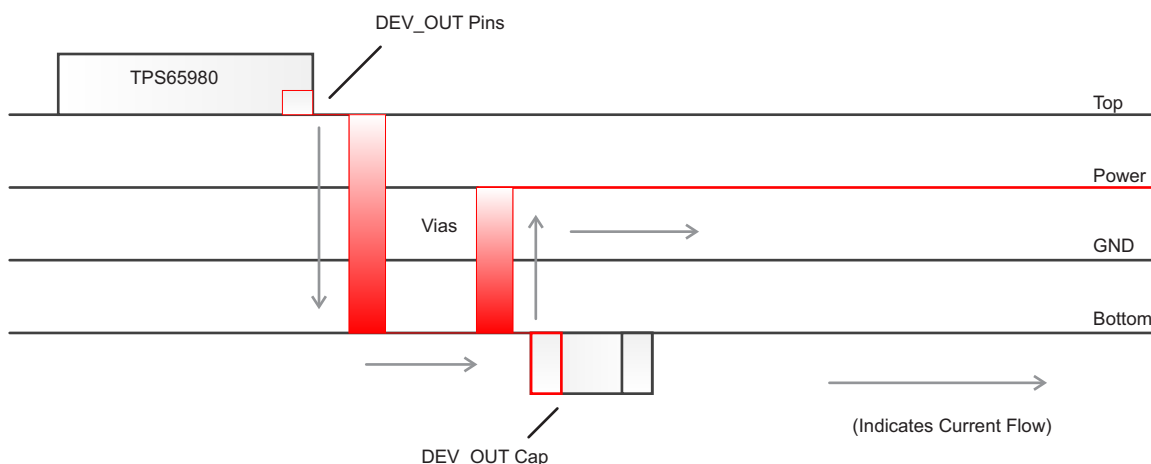


Figure 24. DEV\_OUT Recommended Routing

The charge pump capacitor must be placed on the top layer close to the CPP and CPN pins. The inductance paths from capacitor to the pins must be less than 1 nH. SS and Compensation components should be placed on the top layer close to the device.

## 12 Device and Documentation Support

### 12.1 Trademarks

Thunderbolt is a trademark of Intel Corporation.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary



[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65980RHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS 65980	
TPS65980RHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS 65980	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65980RHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS65980RHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

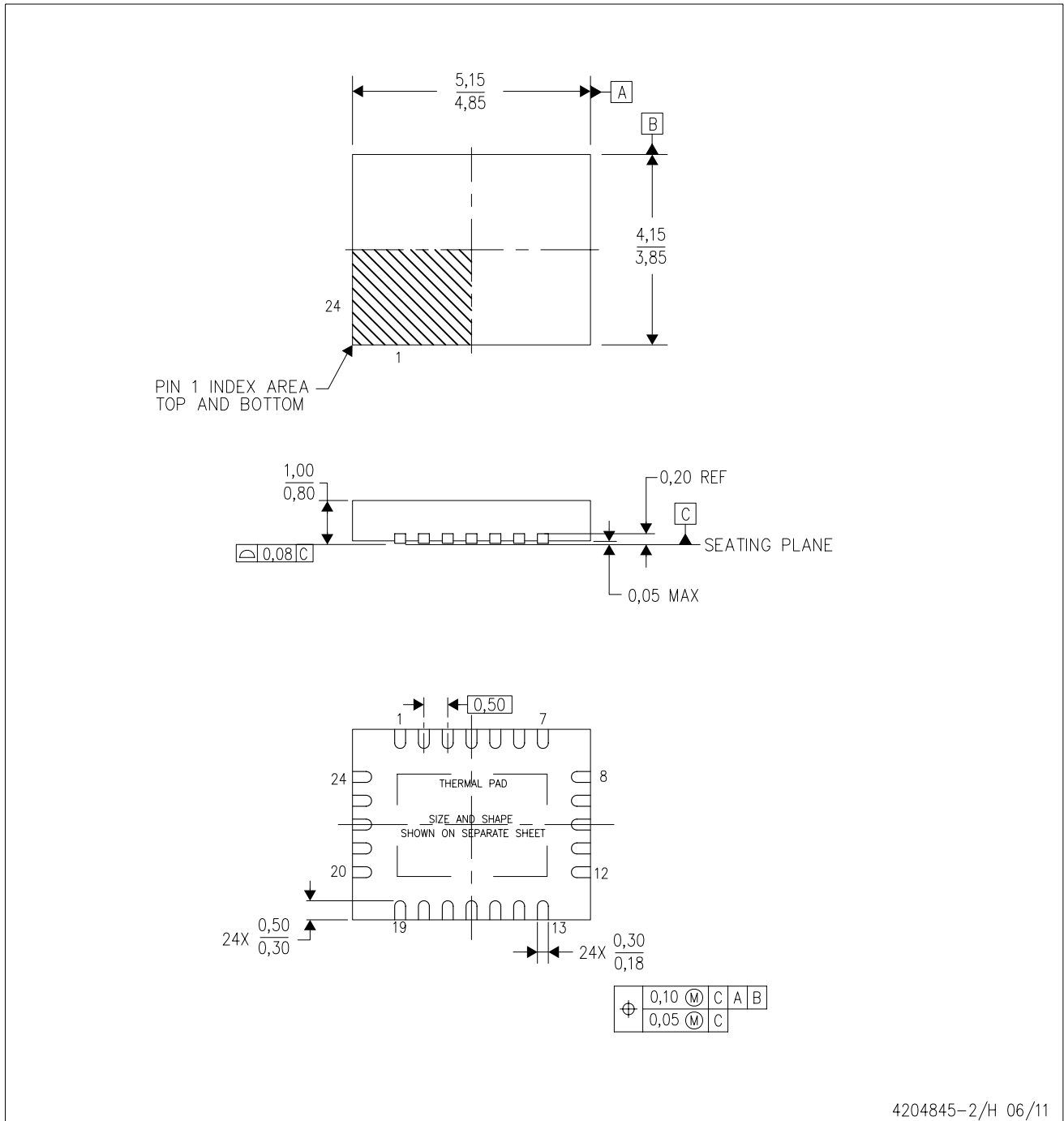

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65980RHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
TPS65980RHFT	VQFN	RHF	24	250	210.0	185.0	35.0

# MECHANICAL DATA

RHF (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204845-2/H 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RHF (R-PVQFN-N24)

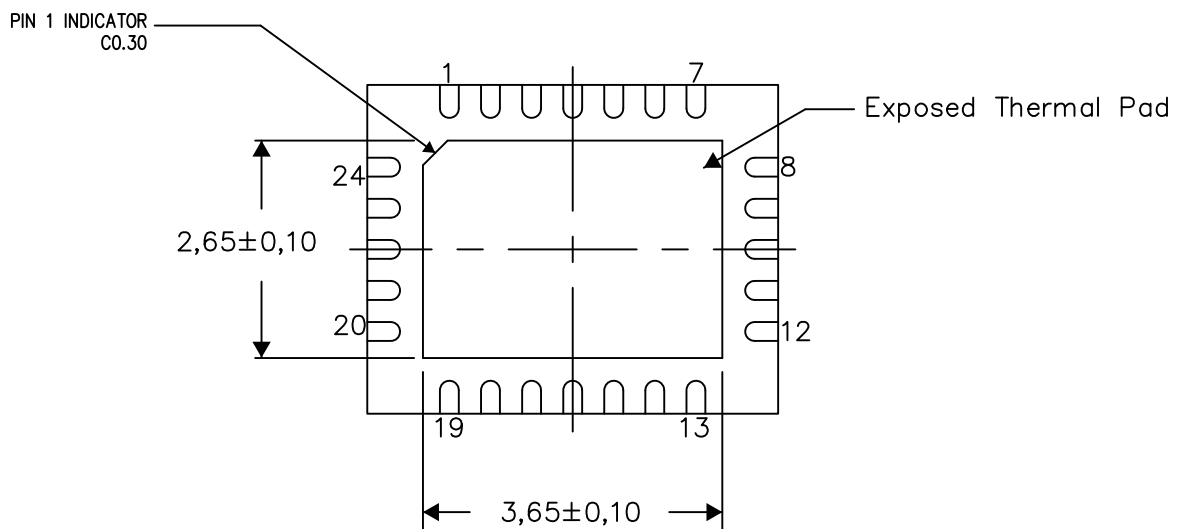
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

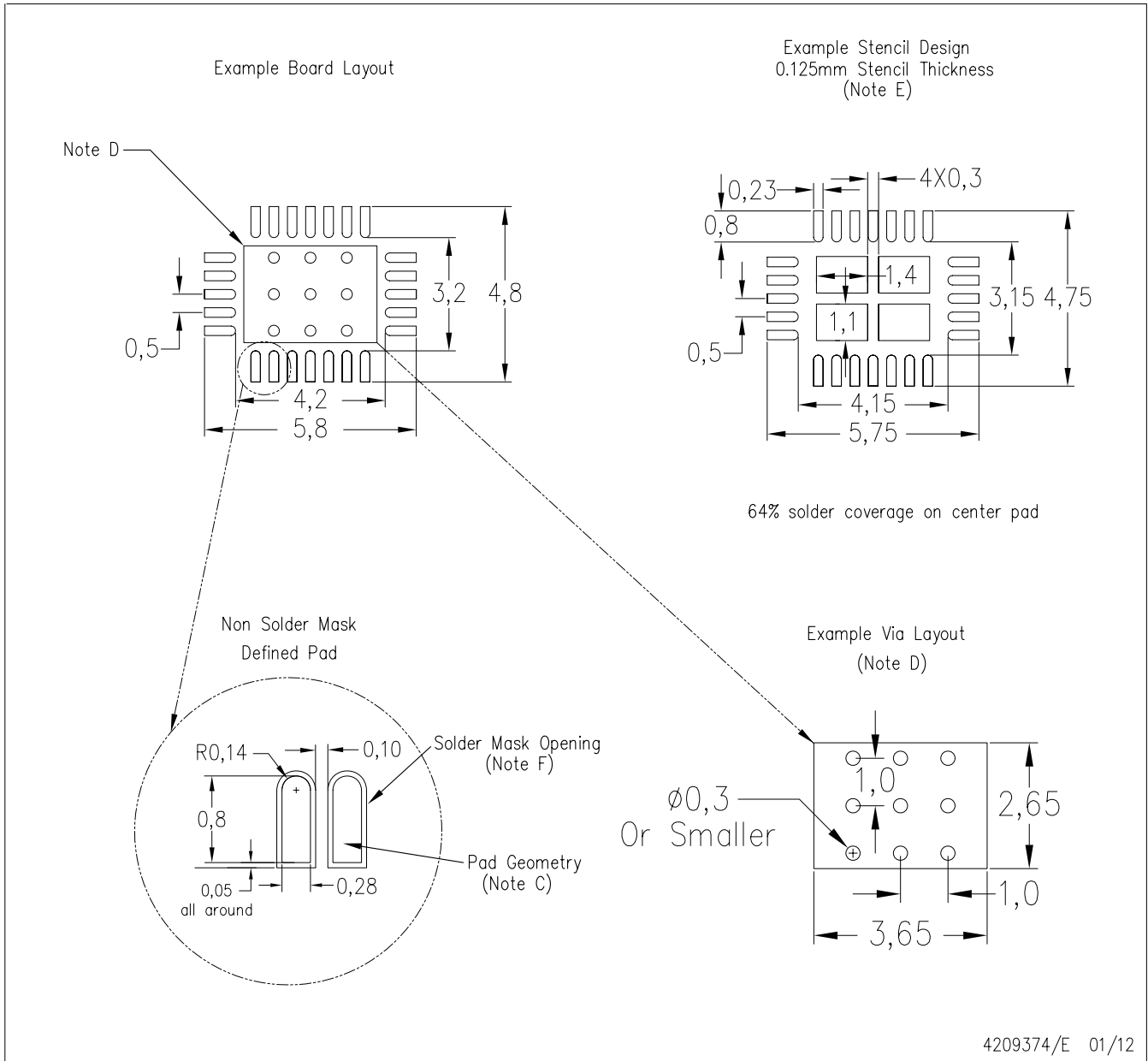
Exposed Thermal Pad Dimensions

4206360-3/K 02/14

NOTE: All linear dimensions are in millimeters

RHF (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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### Applications

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