

ISOW784x High-Performance, 5000-V_{RMS} Reinforced Quad-Channel Digital Isolators With Integrated High-Efficiency, Low-Emissions DC-DC Converter

1 Features

- Integrated High-Efficiency DC-DC Converter With On-Chip Transformer
- 3-V to 5.5-V Wide Input Supply Range
- Regulated 5-V or 3.3-V Output
- Up to 0.65-W Output Power
- 5 V to 5 V; 5 V to 3.3 V: Available Load Current \geq 130 mA
- 3.3 V to 3.3 V: Available Load Current \geq 75 mA
- Soft-Start to Limit Inrush Current
- Overload and Short-Circuit Protection
- Thermal Shutdown
- Default Output: High and Low Options
- Signaling Rate Up to 100 Mbps
- Low Propagation Delay: 13 ns Typ (5-V Supply)
- High CMTI: \pm 100 kV/ μ s Minimum
- Robust Electromagnetic Compatibility (EMC)
 - System-Level ESD, EFT, and Surge Immunity
 - Low Emissions
- 16-pin Wide SOIC Package
- Extended Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Safety-Related Certifications:
 - 7071-V_{PK} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
 - 5000-V_{RMS} Isolation for 1 Minute per UL 1577
 - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
 - CQC Approval per GB4943.1-2011
 - TUV Certification According to EN 60950-1 and EN 61010-1
 - All Agency Certifications are Planned

2 Applications

- Industrial Automation
- Motor Control
- Grid Infrastructure
- Medical Equipment
- Test and Measurement

3 Description

The ISOW784x is a family of high-performance, quad-channel reinforced digital isolators with an integrated high-efficiency power converter. The integrated DC-DC converter provides up to 650 mW of isolated power at high efficiency and can be configured for various input and output voltage configurations. Therefore these devices eliminate the need for a separate isolated power supply in space-constrained isolated designs.

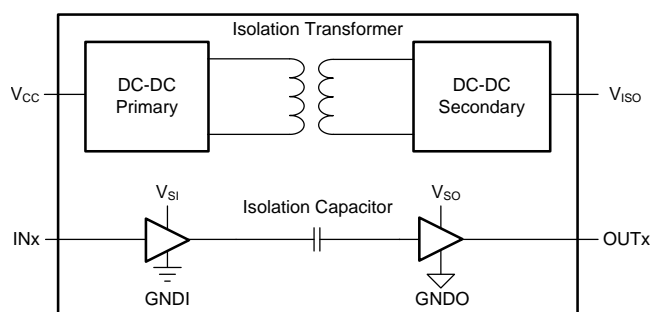
The ISOW784x family of devices provide high electromagnetic immunity and low emissions while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO₂) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. Various configurations of forward and reverse channels are available. If the input signal is lost, the default output is high for the ISOW784x devices and low for the F suffix (see the [Device Features](#)).

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|--|-----------|--------------------|
| ISOW7840 ISOW7841 ISOW7842 ISOW7843 ISOW7844 | SOIC (16) | 10.30 mm x 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



V_{CC} is the primary supply voltage referenced to GND1. V_{ISO} is the isolated supply voltage referenced to GND2.

V_{SI} and V_{SO} can be either V_{CC} or V_{ISO} depending on the channel direction.

V_{SI} is the input-side supply voltage referenced to GND1 and V_{SO} is the output-side supply voltage referenced to GND0.



Table of Contents

| | | | | | |
|----------|---|-----------|-----------|---|-----------|
| 1 | Features | 1 | 7.15 | Insulation Characteristics Curves | 13 |
| 2 | Applications | 1 | 7.16 | Typical Characteristics | 14 |
| 3 | Description | 1 | 8 | Parameter Measurement Information | 18 |
| 4 | Revision History | 2 | 9 | Detailed Description | 19 |
| 5 | Description (continued) | 3 | 9.1 | Overview | 19 |
| 6 | Pin Configuration and Functions | 3 | 9.2 | Functional Block Diagram | 19 |
| 7 | Specifications | 5 | 9.3 | Feature Description | 21 |
| 7.1 | Absolute Maximum Ratings | 5 | 9.4 | Device Functional Modes | 22 |
| 7.2 | ESD Ratings | 5 | 10 | Application and Implementation | 24 |
| 7.3 | Recommended Operating Conditions | 5 | 10.1 | Application Information | 24 |
| 7.4 | Thermal Information | 6 | 10.2 | Typical Application | 24 |
| 7.5 | Power Ratings | 6 | 11 | Power Supply Recommendations | 26 |
| 7.6 | Insulation Specifications | 7 | 12 | Layout | 27 |
| 7.7 | Safety-Related Certifications | 8 | 12.1 | Layout Guidelines | 27 |
| 7.8 | Safety Limiting Values | 8 | 12.2 | Layout Example | 28 |
| 7.9 | DC Electrical Characteristics—5-V Input, 5-V Output | 9 | 13 | Device and Documentation Support | 29 |
| 7.10 | DC Electrical Characteristics—5-V Input, 3.3-V Output | 10 | 13.1 | Documentation Support | 29 |
| 7.11 | DC Electrical Characteristics—3.3-V Input, 3.3-V Output | 11 | 13.2 | Related Links | 29 |
| 7.12 | Switching Characteristics—5-V Input, 5-V Output | 12 | 13.3 | Receiving Notification of Documentation Updates | 29 |
| 7.13 | Switching Characteristics—5-V Input, 3.3-V Output | 12 | 13.4 | Community Resources | 29 |
| 7.14 | Switching Characteristics—3.3-V Input, 3.3-V Output | 12 | 13.5 | Trademarks | 29 |
| | | | 13.6 | Electrostatic Discharge Caution | 29 |
| | | | 13.7 | Glossary | 29 |
| | | | 14 | Mechanical, Packaging, and Orderable Information | 30 |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

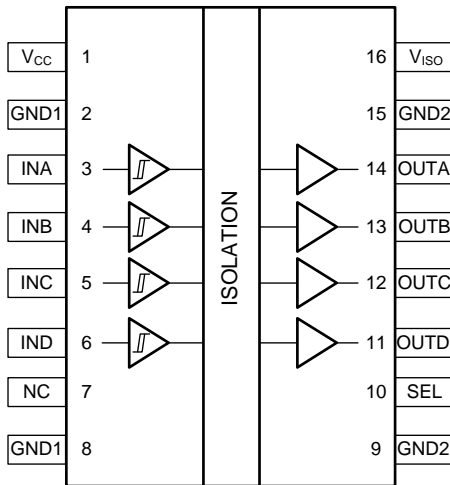
| Changes from Original (March 2017) to Revision A | Page |
|---|-----------|
| • Changed the maximum propagation delay time and the typical and maximum values for pulse width distortion in all <i>Switching Characteristics</i> tables | 12 |
| • Changed the maximum limit for output signal rise and fall times from 3 to 4 ns in the <i>Switching Characteristics—5-V Input, 3.3-V Output</i> table | 12 |

5 Description (continued)

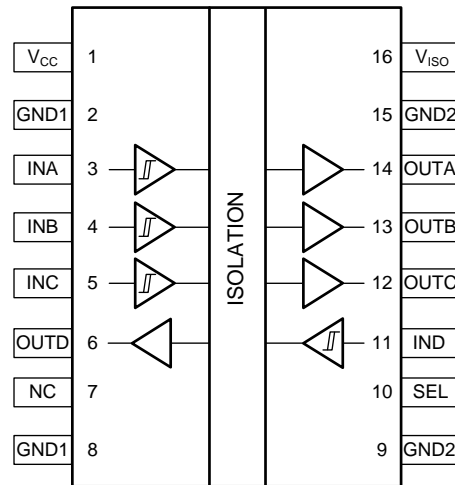
These devices help prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISOW784x family of devices has been significantly enhanced to ease system-level ESD, EFT, surge and emissions compliance. The high-efficiency of the power converter allows operation at a higher ambient temperature. The ISOW784x family of devices is available in a 16-pin SOIC wide-body (SOIC-WB) DWE package.

6 Pin Configuration and Functions

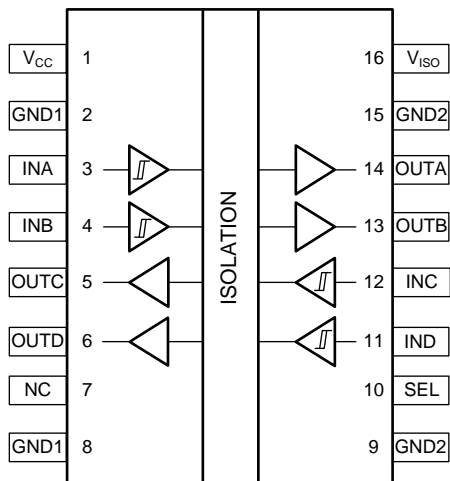
ISOW7840 DWE Package
16-Pin SOIC-WB
Top View



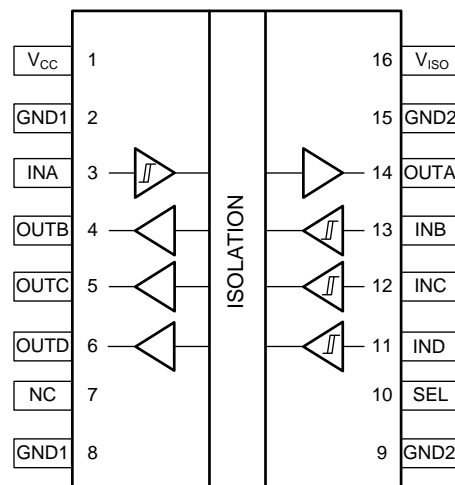
ISOW7841 DWE Package
16-Pin SOIC-WB
Top View

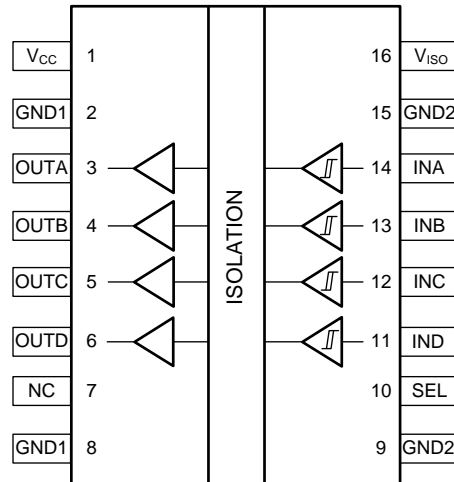


ISOW7842 DWE Package
16-Pin SOIC-WB
Top View



ISOW7843 DWE Package
16-Pin SOIC-WB
Top View



**ISOW7844 DWE Package
16-Pin SOIC-WB
Top View**

Pin Functions

| NAME | PIN NO. | | | | | I/O | DESCRIPTION |
|-----------|----------|----------|----------|----------|----------|-----|---|
| | ISOW7840 | ISOW7841 | ISOW7842 | ISOW7843 | ISOW7844 | | |
| GND1 | 2, 8 | 2, 8 | 2, 8 | 2, 8 | 2, 8 | — | Ground connection for V_{CC} |
| GND2 | 9, 15 | 9, 15 | 9, 15 | 9, 15 | 9, 15 | — | Ground connection for V_{ISO} |
| INA | 3 | 3 | 3 | 3 | 14 | I | Input channel A |
| INB | 4 | 4 | 4 | 13 | 13 | I | Input channel B |
| INC | 5 | 5 | 12 | 12 | 12 | I | Input channel C |
| IND | 6 | 11 | 11 | 11 | 11 | I | Input channel D |
| NC | 7 | 7 | 7 | 7 | 7 | — | Not connected |
| OUTA | 14 | 14 | 14 | 14 | 3 | O | Output channel A |
| OUTB | 13 | 13 | 13 | 4 | 4 | O | Output channel B |
| OUTC | 12 | 12 | 5 | 5 | 5 | O | Output channel C |
| OUTD | 11 | 6 | 6 | 6 | 6 | O | Output channel D |
| SEL | 10 | 10 | 10 | 10 | 10 | I | V_{ISO} selection pin. $V_{ISO} = 5\text{ V}$ when SEL shorted to V_{ISO} . $V_{ISO} = 3.3\text{ V}$, when SEL shorted to GND2 or when left floating. For more information see the Device Functional Modes . |
| V_{CC} | 1 | 1 | 1 | 1 | 1 | — | Supply voltage |
| V_{ISO} | 16 | 16 | 16 | 16 | 16 | — | Isolated supply voltage determined by SEL pin |

7 Specifications

7.1 Absolute Maximum Ratings

 See ⁽¹⁾⁽²⁾

| | | MIN | MAX | UNIT |
|-----------|--|------|--|------|
| V_{CC} | Supply voltage | -0.5 | 6 | V |
| V_{ISO} | Isolated supply voltage | -0.5 | 6 | V |
| V_{IO} | Voltage at INx, OUTx, SEL pins | -0.5 | $V_{CC} + 0.5,$ $V_{ISO} + 0.5^{(3)}$ | V |
| I_O | Maximum output current through data channels | -15 | 15 | mA |
| T_J | Junction temperature | | 150 | °C |
| T_{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.
- (3) This value depends on whether the pin is located on the V_{CC} or V_{ISO} side. The maximum voltage at the I/O pins should not exceed 6 V.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|----------|--|-----------------------------|-----|---------------------|------|
| V_{CC} | Supply voltage | 3 | | 5.5 | V |
| I_{OH} | High level output current ⁽²⁾ | $V_{SO}^{(1)} = 5\text{ V}$ | -4 | | mA |
| | | $V_{SO} = 3.3\text{ V}$ | -2 | | |
| I_{OL} | Low level output current ⁽²⁾ | $V_{SO} = 5\text{ V}$ | | 4 | mA |
| | | $V_{SO} = 3.3\text{ V}$ | | 2 | |
| V_{IH} | High-level input voltage | $0.7 \times V_{SI}$ | | V_{SI} | V |
| V_{IL} | Low-level input voltage | 0 | | $0.3 \times V_{SI}$ | V |
| DR | Data rate | | | 100 | Mbps |
| T_J | Junction temperature | -40 | | 150 | °C |
| T_A | Ambient temperature | -40 | | 125 | °C |

- (1) V_{SI} is the input side supply, V_{SO} is the output side supply
- (2) This current is for data output channel.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | ISOW784x | UNIT |
|-------------------------------|--|------------|------|
| | | DWE (SOIC) | |
| | | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 56.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 15.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 28.5 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 2.4 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 28.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Power Ratings

$V_{CC} = 5.5\text{ V}$, $I_{ISO} = 110\text{ mA}$, $T_J = 150^\circ\text{C}$, $T_A \leq 80^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50-MHz 50% duty-cycle square wave

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|-----------------|-----|-----|------|------|
| P_D | Maximum power dissipation (both sides) | | | | 1.02 | W |
| P_{D1} | Maximum power dissipation (side-1) | | | | 0.51 | W |
| P_{D2} | Maximum power dissipation (side-2) | | | | 0.51 | W |

7.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|--------------------|------------------|
| GENERAL | | | | |
| CLR | External clearance ⁽¹⁾ | Shortest terminal-to-terminal distance through air | >8 | mm |
| CPG | External creepage ⁽¹⁾ | Shortest terminal-to-terminal distance across the package surface | >8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance – capacitive signal isolation) | > 21 | µm |
| | | Minimum internal gap (internal clearance – transformer power isolation) | >120 | |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | > 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 300 V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 600 V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 1000 V _{RMS} | I-III | |
| DIN V VDE 0884-10 (VDE V 0884-10): 2016-12⁽²⁾ | | | | |
| V _{IORM} | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1414 | V _{PK} |
| V _{IOWM} | Maximum isolation working voltage | AC voltage; Time dependent dielectric breakdown (TDDB) Test | 1000 | V _{RMS} |
| | | DC voltage | 1414 | V _{DC} |
| V _{IOTM} | Maximum transient isolation voltage | V _{TEST} = V _{IOTM} ; t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} ; t = 1 s (100% production) | 7071 | V _{PK} |
| V _{IOSM} | Maximum surge isolation voltage ⁽³⁾ | Test method per IEC 60065, 1.2/50 µs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification) | 6250 | V _{PK} |
| q _{pd} | Apparent charge ⁽⁴⁾ | Method a, after input/output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s | ≤ 5 | pC |
| | | Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s | ≤ 5 | |
| | | Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s | ≤ 5 | |
| C _{IO} | Barrier capacitance, input to output ⁽⁵⁾ | V _{IO} = 0.4 × sin(2πft), f = 1 MHz | ~3.5 | pF |
| R _{IO} | Insulation resistance ⁽⁵⁾ | V _{IO} = 500 V, T _A = 25°C | > 10 ¹² | Ω |
| | | V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C | > 10 ¹¹ | |
| | | V _{IO} = 500 V, T _S = 150°C | > 10 ⁹ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| UL 1577 | | | | |
| V _{ISO(UL)} | Withstand isolation voltage | V _{TEST} = V _{ISO(UL)} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO(UL)} , t = 1 s (100% production) | 5000 | V _{RMS} |

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

All certifications are planned.

| VDE | CSA | UL | CQC | TUV |
|--|---|--|---|---|
| Plan to certify according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 | Plan to certify under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 | Plan to certify according to UL 1577 Component Recognition Program | Plan to certify according to GB 4943.1-2011 | Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010 /A 12:2011/A2:2013 |
| Maximum transient isolation voltage, 7071 V_{PK} ; Maximum repetitive peak isolation voltage, 1414 V_{PK} ; Maximum surge isolation voltage, 6250 V_{PK} | Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} maximum working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} maximum working voltage | Single protection, 5000 V_{RMS} | Reinforced Insulation, Altitude \leq 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage; | 5000 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010 /A 12:2011/A2:2013 up to working voltage of 800 V_{RMS} |
| Certificate planned | Certificate planned | Certificate planned | Certificate planned | Certificate planned |

7.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|------|------------------|
| I_S Safety input, output, or supply current | $R_{\theta JA} = 56.8^\circ\text{C/W}$, $V_I = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$, see Figure 1 | | | 400 | mA |
| | $R_{\theta JA} = 56.8^\circ\text{C/W}$, $V_I = 3.6\text{ V}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$, see Figure 1 | | | 611 | |
| P_S Safety input, output, or total power | $R_{\theta JA} = 56.8^\circ\text{C/W}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$, see Figure 2 | | | 2200 | mW |
| T_S Maximum safety temperature | | | | 150 | $^\circ\text{C}$ |

- (1) The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance. For more information see the [Thermal Information](#) section.

7.9 DC Electrical Characteristics—5-V Input, 5-V Output

These specifications are for the ISOW7841 and ISOW7841F devices only; $V_{CC} = 5\text{ V} \pm 10\%$, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|----------------------|----------------|------|---------------|
| I_{CC} Current drawn from supply | No external I_{ISO} ; $V_I = 0\text{ V}$ (ISOW7841); $V_I = V_{SI}^{(1)}$ (ISOW7841 with F suffix) | | 23 | | mA |
| | No external I_{ISO} ; $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | | 17 | | |
| | All channels switching with square wave clock input of 0.5 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 20 | | |
| | All channels switching with square wave clock input of 5 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 24 | | |
| | All channels switching with square wave clock input of 50 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 54 | | |
| $I_{ISO(OUT)}^{(2)}$ Current available to isolated supply | $V_I = 0\text{ V}$ (ISOW7841); $V_I = V_{SI}$ (ISOW7841 with F suffix) | 128 | | | mA |
| | $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | 130 | | | |
| | All channels switching with square wave clock input of 0.5 MHz; $C_L = 15\text{ pF}$ | 128 | | | |
| | All channels switching with square wave clock input of 5 MHz; $C_L = 15\text{ pF}$ | 127 | | | |
| | All channels switching with square wave clock input of 50 MHz; $C_L = 15\text{ pF}$ | 112 | | | |
| V_{ISO} Isolated supply voltage | External $I_{ISO} = 0$ to 50 mA | 4.75 | 5.07 | 5.43 | V |
| | External $I_{ISO} = 0$ to 130 mA | 4.5 | 5.07 | 5.43 | |
| $V_{ISO(LINE)}$ DC line regulation | $I_{ISO} = 50\text{ mA}$, $V_{CC} = 4.5\text{ V}$ to 5.5 V | | 2 | | mV/V |
| $V_{ISO(LOAD)}$ DC load regulation | $I_{ISO} = 0$ to 130 mA | | 1% | | |
| EFF Efficiency at maximum load current | $I_{ISO} = 130\text{ mA}$, $C_{LOAD} = 0.1\text{ }\mu\text{F} \parallel 10\text{ }\mu\text{F}$; $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | | 53% | | |
| $V_{CC+(UVLO)}$ Positive-going UVLO threshold on V_{CC} , V_{ISO} | | | | 2.7 | V |
| $V_{CC-(UVLO)}$ Negative-going UVLO threshold on V_{CC} , V_{ISO} | | 2.1 | | | V |
| $V_{HYS(UVLO)}$ UVLO threshold hysteresis on V_{CC} , V_{ISO} | | | 0.2 | | V |
| V_{ITH} Input pin rising threshold | | | | 0.7 | V_{SI} |
| V_{ITL} Input pin falling threshold | | 0.3 | | | V_{SI} |
| $V_{I(HYS)}$ Input pin threshold hysteresis (INx) | | 0.1 | | | V_{SI} |
| I_{IL} Low level input current | $V_{IL} = 0$ at INx or SEL | -10 | | | μA |
| I_{IH} High level input current | $V_{IH} = V_{SI}^{(1)}$ at INx or SEL | | | 10 | μA |
| V_{OH} High level output voltage | $I_O = -4\text{ mA}$, see Figure 24 | $V_{SO}^{(1)} - 0.4$ | $V_{SO} - 0.2$ | | V |
| V_{OL} Low level output voltage | $I_O = 4\text{ mA}$, see Figure 24 | | 0.2 | 0.4 | V |
| CMTI Common mode transient immunity | $V_I = V_{SI}$ or 0 V , $V_{CM} = 1000\text{ V}$; see Figure 25 | 100 | | | kV/us |
| I_{CC_SC} DC current from supply under short circuit on V_{ISO} | V_{ISO} shorted to GND2 | | 137 | | mA |
| $V_{ISO(RIP)}$ Output ripple on isolated supply (pk-pk) | 20-MHz bandwidth, $C_{LOAD} = 0.1\text{ }\mu\text{F} \parallel 20\text{ }\mu\text{F}$, $I_{ISO} = 130\text{ mA}$ | | 100 | | mV |

(1) V_{SI} = input side supply; V_{SO} = output side supply

(2) Current available to load should be derated by $2\text{ mA}/^\circ\text{C}$ for $T_A > 80^\circ\text{C}$.

7.10 DC Electrical Characteristics—5-V Input, 3.3-V Output

These specifications are for the ISOW7841 and ISOW7841F devices only; $V_{CC} = 5\text{ V} \pm 10\%$, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|----------------------|----------------|------|---------------|
| I_{CC} Current drawn from supply | No external I_{ISO} ; $V_I = 0\text{ V}$ (ISOW7841); $V_I = V_{SI}^{(1)}$ (ISOW7841 with F suffix) | | 20 | | mA |
| | No external I_{ISO} ; $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | | 14 | | |
| | All channels switching with square wave clock input of 0.5 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 17 | | |
| | All channels switching with square wave clock input of 5 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 20 | | |
| | All channels switching with square wave clock input of 50 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 40 | | |
| $I_{ISO(OUT)}^{(2)}$ Current available to isolated supply | $V_I = 0\text{ V}$ (ISOW7841); $V_I = V_{SI}$ (ISOW7841 with F suffix) | 128 | | | mA |
| | $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | 130 | | | |
| | All channels switching with square wave clock input of 0.5 MHz; $C_L = 15\text{ pF}$ | 129 | | | |
| | All channels switching with square wave clock input of 5 MHz; $C_L = 15\text{ pF}$ | 128 | | | |
| | All channels switching with square wave clock input of 50 MHz; $C_L = 15\text{ pF}$ | 118 | | | |
| V_{ISO} Isolated supply voltage | External $I_{ISO} = 0$ to 50 mA | 3.13 | 3.34 | 3.56 | V |
| | External $I_{ISO} = 0$ to 130 mA | 3 | 3.34 | 3.56 | |
| $V_{ISO(LINE)}$ DC line regulation | $I_{ISO} = 50\text{ mA}$, $V_{CC} = 4.5\text{ V}$ to 5.5 V | | 2 | | mV/V |
| $V_{ISO(LOAD)}$ DC load regulation | $I_{ISO} = 10$ to 130 mA | | 1% | | |
| EFF Efficiency at maximum load current | $I_{ISO} = 130\text{ mA}$, $C_{LOAD} = 0.1\text{ }\mu\text{F} \parallel 10\text{ }\mu\text{F}$; $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | | 48% | | |
| $V_{CC+(UVLO)}$ Positive-going UVLO threshold on V_{CC} , V_{ISO} | | | | 2.7 | V |
| $V_{CC-(UVLO)}$ Negative-going UVLO threshold on V_{CC} , V_{ISO} | | 2.1 | | | V |
| $V_{HYS(UVLO)}$ UVLO threshold hysteresis on V_{CC} , V_{ISO} | | | 0.2 | | V |
| V_{ITH} Input pin rising threshold | | | | 0.7 | V_{SI} |
| V_{ITL} Input pin falling threshold | | 0.3 | | | V_{SI} |
| $V_{I(HYS)}$ Input pin threshold hysteresis (INx) | | 0.1 | | | V_{SI} |
| I_{IL} Low level input current | $V_{IL} = 0$ at INx or SEL | -10 | | | μA |
| I_{IH} High level input current | $V_{IH} = V_{SI}^{(1)}$ at INx or SEL | | | 10 | μA |
| V_{OH} High level output voltage | $I_O = -2\text{ mA}$, see Figure 24 | $V_{SO}^{(1)} - 0.3$ | $V_{SO} - 0.1$ | | V |
| V_{OL} Low level output voltage | $I_O = 2\text{ mA}$, see Figure 24 | | 0.1 | 0.3 | V |
| CMTI Common mode transient immunity | $V_I = V_{SI}$ or 0 V , $V_{CM} = 1000\text{ V}$; see Figure 25 | 100 | | | kV/us |
| I_{CC_SC} DC current from supply under short circuit on V_{ISO} | V_{ISO} shorted to GND2 | | 137 | | mA |
| $V_{ISO(RIP)}$ Output ripple on isolated supply (pk-pk) | 20-MHz bandwidth, $C_{LOAD} = 0.1\text{ }\mu\text{F} \parallel 20\text{ }\mu\text{F}$, $I_{ISO} = 130\text{ mA}$ | | 100 | | mV |

(1) V_{SI} = input side supply; V_{SO} = output side supply

(2) Current available to load should be derated by $2\text{ mA}/^\circ\text{C}$ for $T_A > 105^\circ\text{C}$.

7.11 DC Electrical Characteristics—3.3-V Input, 3.3-V Output

These specifications are for the ISOW7841 and ISOW7841F devices only; $V_{CC} = 3.3\text{ V} \pm 10\%$, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|--|----------------------|----------------|------|---------------|
| I_{CC} | Current drawn from supply | No external I_{ISO} ; $V_I = 0\text{ V}$ (ISOW7841); $V_I = V_S^{(1)}$ (ISOW7841 with F suffix) | | 26 | | mA |
| | | No external I_{ISO} ; $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | | 20 | | |
| | | All channels switching with square wave clock input of 0.5 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 23 | | |
| | | All channels switching with square wave clock input of 5 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 26 | | |
| | | All channels switching with square wave clock input of 50 MHz; $C_L = 15\text{ pF}$, No external I_{ISO} | | 53 | | |
| $I_{ISO(OUT)}^{(2)}$ | Current available to isolated supply | $V_I = 0\text{ V}$ (ISOW7841); $V_I = V_{SI}$ (ISOW7841 with F suffix) | 73 | | | mA |
| | | $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | 75 | | | |
| | | All channels switching with square wave clock input of 0.5 MHz; $C_L = 15\text{ pF}$ | 74 | | | |
| | | All channels switching with square wave clock input of 5 MHz; $C_L = 15\text{ pF}$ | 73 | | | |
| | | All channels switching with square wave clock input of 50 MHz; $C_L = 15\text{ pF}$ | 61 | | | |
| V_{ISO} | Isolated supply voltage | External $I_{ISO} = 0$ to 30 mA | 3.13 | 3.34 | 3.58 | V |
| | | External $I_{ISO} = 0$ to 75 mA | 3 | 3.34 | 3.58 | |
| $V_{ISO(LINE)}$ | DC line regulation | $I_{ISO} = 30\text{ mA}$, $V_{CC} = 3\text{ V}$ to 3.6 V | | 2 | | mV/V |
| $V_{ISO(LOAD)}$ | DC load regulation | $I_{ISO} = 0$ to 75 mA | | 1% | | |
| EFF | Efficiency at maximum load current | $I_{ISO} = 75\text{ mA}$, $C_{LOAD} = 0.1\text{ }\mu\text{F} \parallel 10\text{ }\mu\text{F}$; $V_I = V_{SI}$ (ISOW7841); $V_I = 0\text{ V}$ (ISOW7841 with F suffix) | | 47% | | |
| $V_{CC+(UVLO)}$ | Positive-going UVLO threshold on V_{CC} , V_{ISO} | | | | 2.7 | V |
| $V_{CC-(UVLO)}$ | Negative-going UVLO threshold on V_{CC} , V_{ISO} | | 2.1 | | | V |
| $V_{HYS (UVLO)}$ | UVLO threshold hysteresis on V_{CC} , V_{ISO} | | | 0.2 | | V |
| V_{ITH} | Input pin rising threshold | | | | 0.7 | V_{SI} |
| V_{ITL} | Input pin falling threshold | | 0.3 | | | V_{SI} |
| $V_{I(HYS)}$ | Input pin threshold hysteresis (INx) | | 0.1 | | | V_{SI} |
| I_{IL} | Low level input current | $V_{IL} = 0$ at INx or SEL | -10 | | | μA |
| I_{IH} | High level input current | $V_{IH} = V_{SI}^{(1)}$ at INx or SEL | | | 10 | μA |
| V_{OH} | High level output voltage | $I_O = -2\text{ mA}$, see Figure 24 | $V_{SO}^{(1)} - 0.3$ | $V_{SO} - 0.1$ | | V |
| V_{OL} | Low level output voltage | $I_O = 2\text{ mA}$, see Figure 24 | | 0.1 | 0.3 | V |
| CMTI | Common mode transient immunity | $V_I = V_{SI}$ or 0 V, $V_{CM} = 1000\text{ V}$; see Figure 25 | 100 | | | kV/us |
| I_{CC_SC} | DC current from supply under short circuit on V_{ISO} | V_{ISO} shorted to GND2 | | 143 | | mA |
| $V_{ISO(RIP)}$ | Output ripple on isolated supply (pk-pk) | 20-MHz bandwidth, $C_{LOAD} = 0.1\text{ }\mu\text{F} \parallel 20\text{ }\mu\text{F}$, $I_{ISO} = 75\text{ mA}$ | | 90 | | mV |

(1) V_{SI} = input side supply; V_{SO} = output side supply

(2) Current available to load should be derated by 2 mA/°C for $T_A > 115^\circ\text{C}$.

7.12 Switching Characteristics—5-V Input, 5-V Output

These specifications are for the ISOW7841 and ISOW7841F devices only; $V_{CC} = 5\text{ V} \pm 10\%$, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------------------|-----|-----|------|------|
| t_{PLH} , t_{PHL} Propagation delay time | See Figure 24 | | 13 | 17.6 | ns |
| PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $ | | | 0.6 | 4.7 | ns |
| $t_{SK(o)}$ Channel-channel output skew time ⁽²⁾ | Same-direction channels | | | 2.5 | ns |
| $t_{SK(p-p)}$ Part-part skew time ⁽³⁾ | | | | 4.5 | ns |
| t_r , t_f Output signal rise and fall times | | | 2 | 4 | ns |

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.13 Switching Characteristics—5-V Input, 3.3-V Output

These specifications are for the ISOW7841 and ISOW7841F devices only; $V_{CC} = 5\text{ V} \pm 10\%$, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------------------|-----|-----|------|------|
| t_{PLH} , t_{PHL} Propagation delay time | See Figure 24 | | 14 | 19.7 | ns |
| PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $ | | | 0.6 | 4.4 | ns |
| $t_{SK(o)}$ Channel-channel output skew time ⁽²⁾ | Same-direction channels | | | 2 | ns |
| $t_{SK(p-p)}$ Part-part skew time ⁽³⁾ | | | | 4.5 | ns |
| t_r , t_f Output signal rise and fall times | | | 1 | 4 | ns |

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

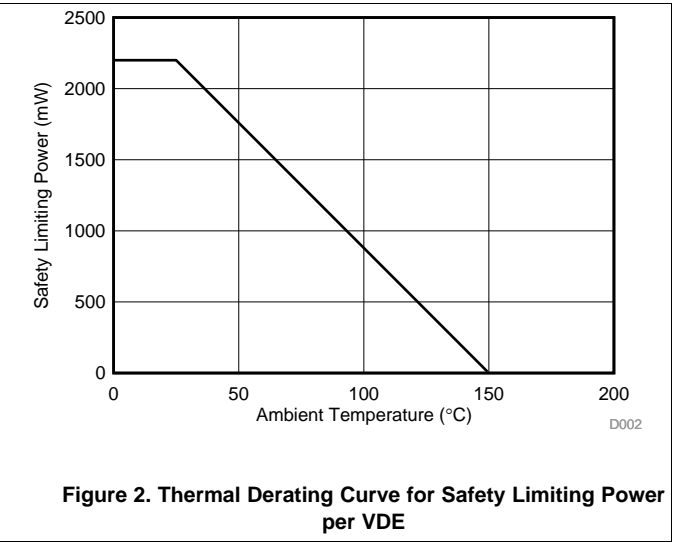
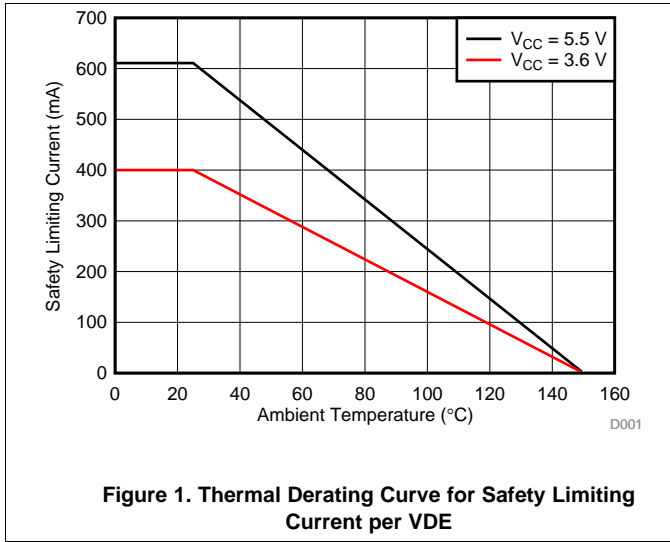
7.14 Switching Characteristics—3.3-V Input, 3.3-V Output

These specifications are for the ISOW7841 and ISOW7841F devices only; $V_{CC} = 3.3\text{ V} \pm 10\%$, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------------------|-----|------|------|------|
| t_{PLH} , t_{PHL} Propagation delay time | See Figure 24 | | 14.5 | 20.2 | ns |
| PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $ | | | 0.6 | 4.4 | ns |
| $t_{SK(o)}$ Channel-channel output skew time ⁽²⁾ | Same-direction channels | | | 2.2 | ns |
| $t_{SK(p-p)}$ Part-part skew time ⁽³⁾ | | | | 4.5 | ns |
| t_r , t_f Output signal rise and fall times | | | 1 | 3 | ns |

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.15 Insulation Characteristics Curves



7.16 Typical Characteristics

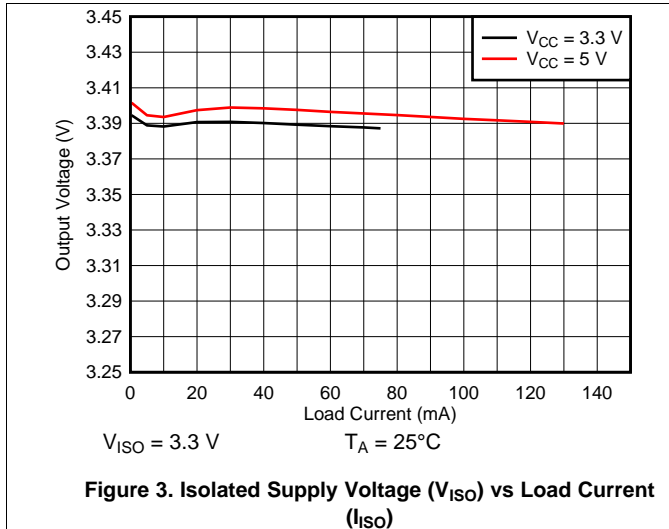


Figure 3. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})

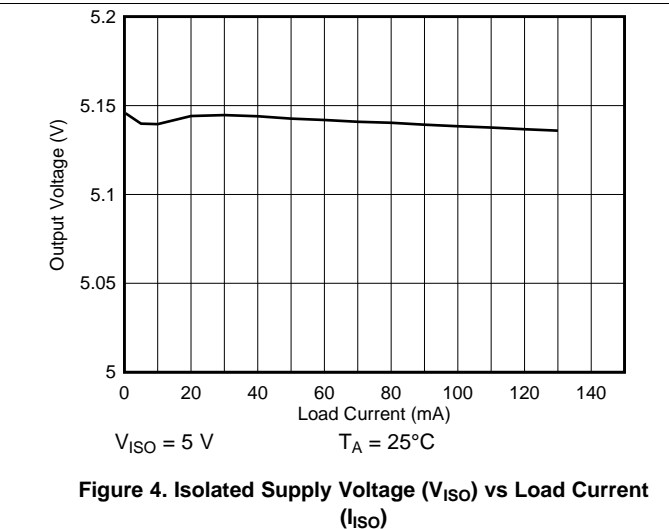


Figure 4. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})

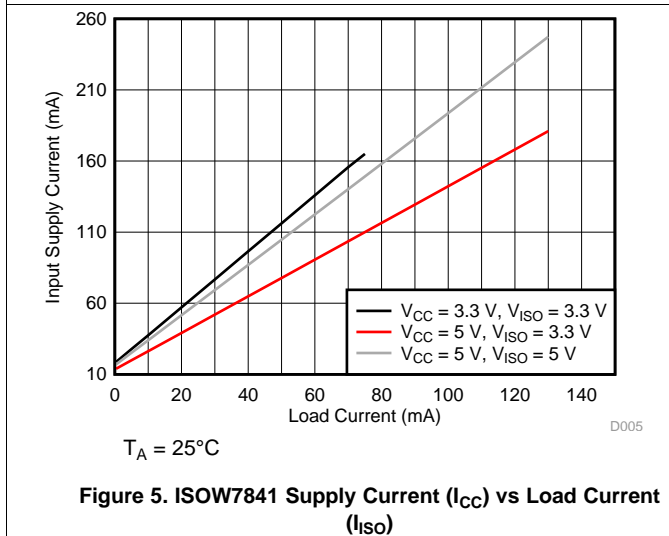


Figure 5. ISOW7841 Supply Current (I_{CC}) vs Load Current (I_{ISO})

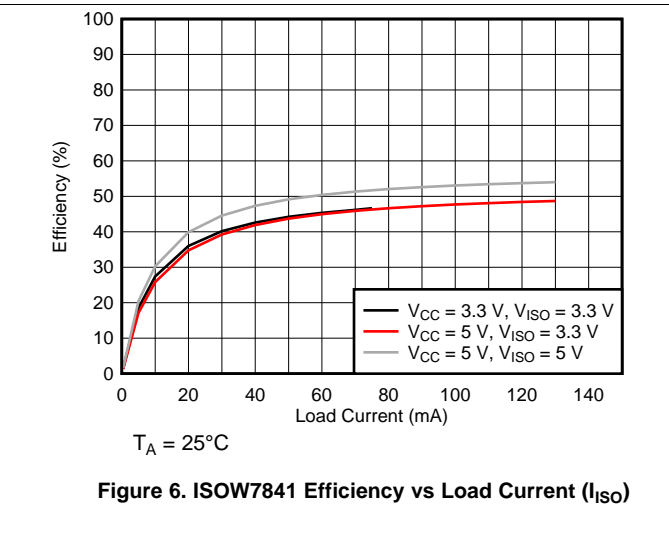


Figure 6. ISOW7841 Efficiency vs Load Current (I_{ISO})

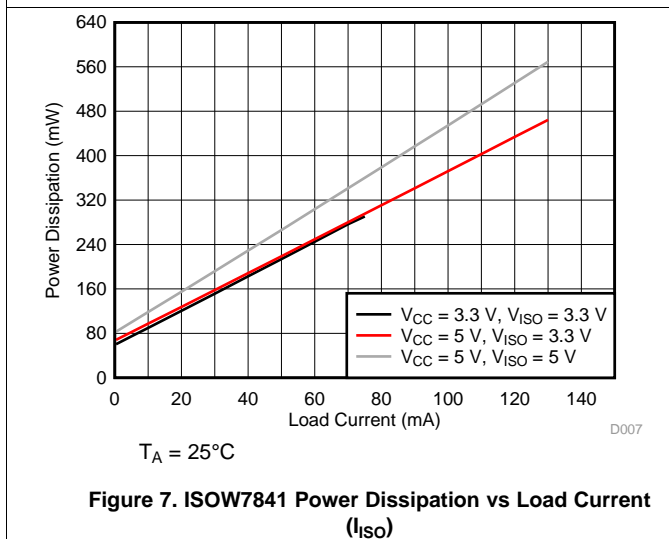


Figure 7. ISOW7841 Power Dissipation vs Load Current (I_{ISO})

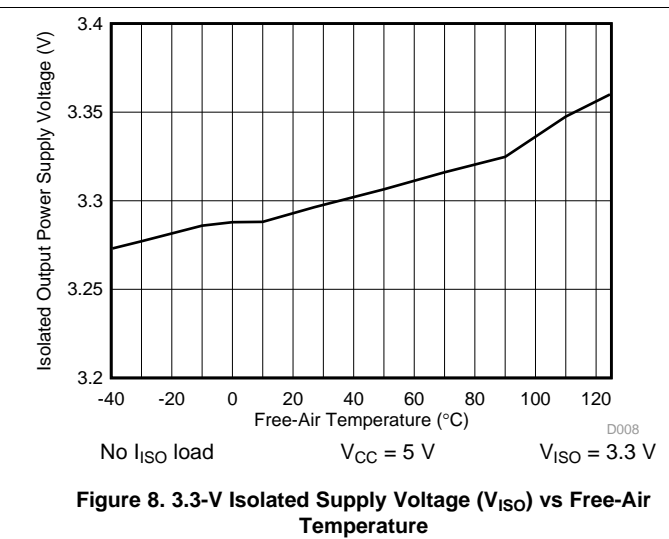
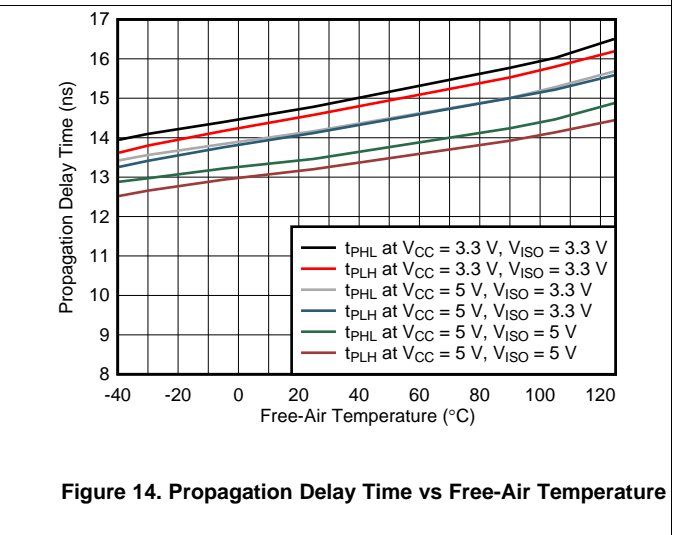
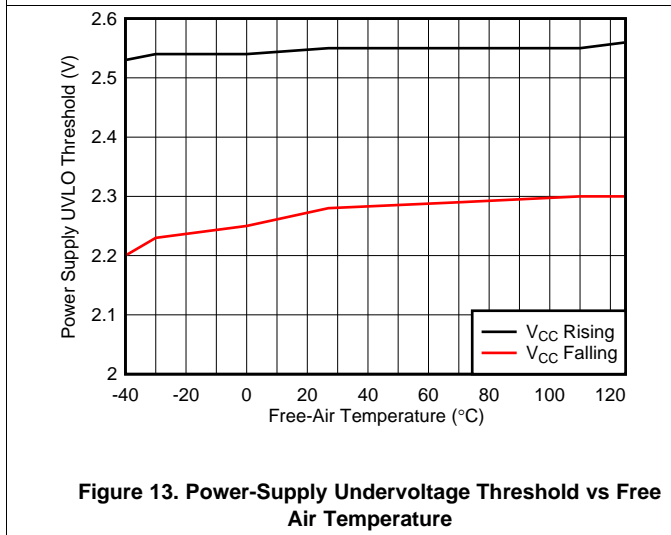
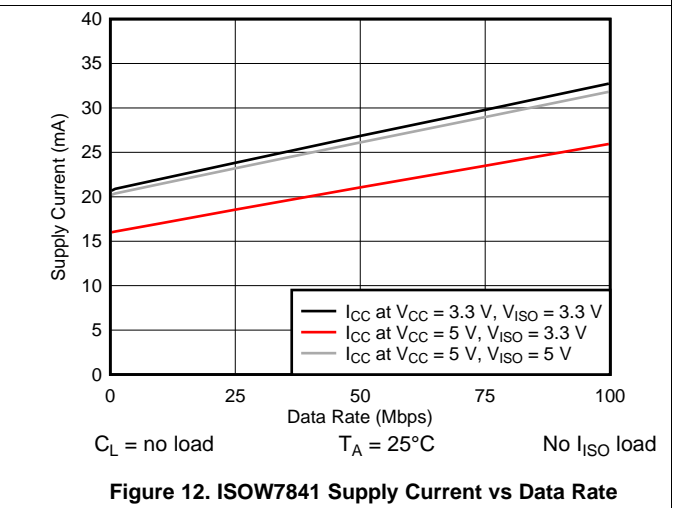
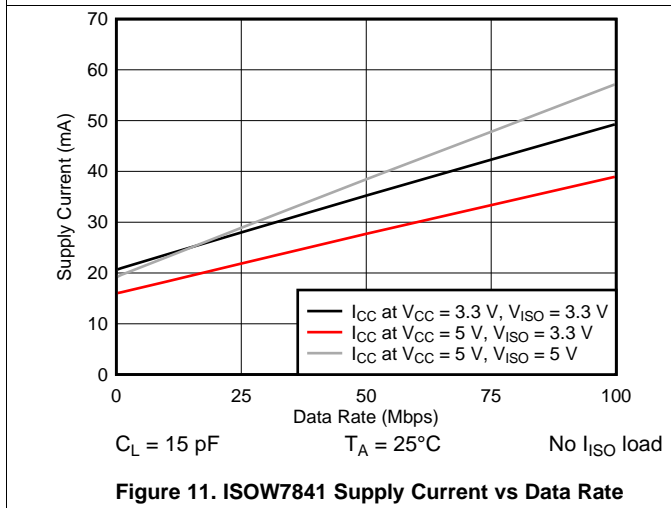
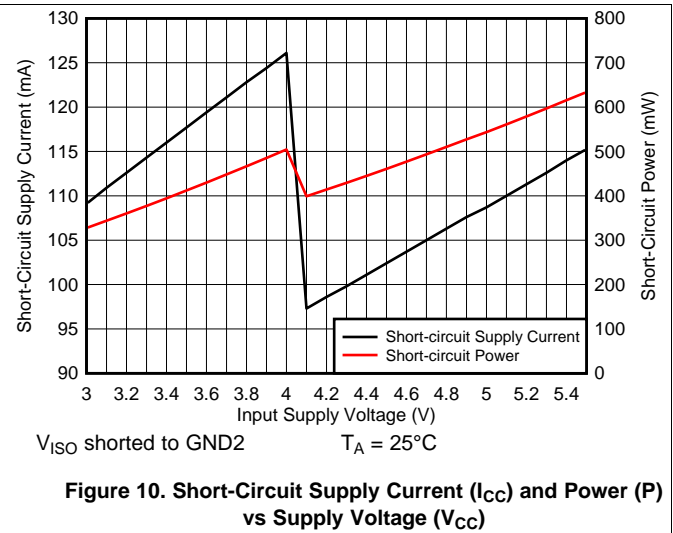
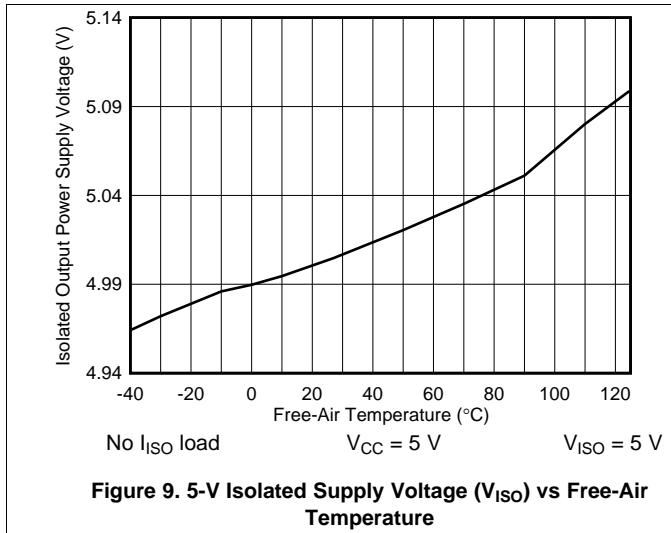


Figure 8. 3.3-V Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature

Typical Characteristics (continued)



Typical Characteristics (continued)

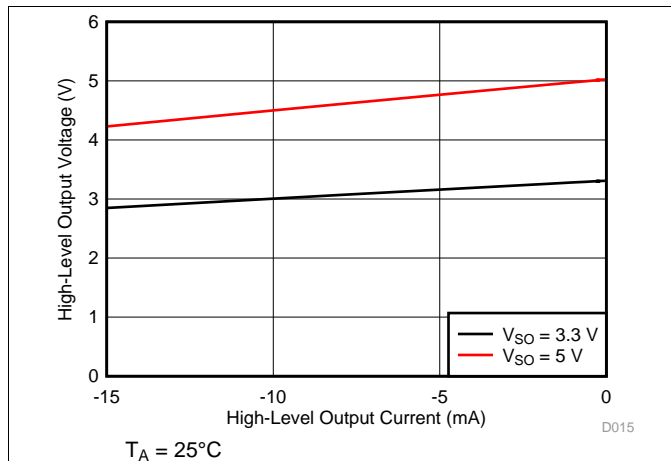


Figure 15. High-Level Output Voltage vs High-Level Output Current

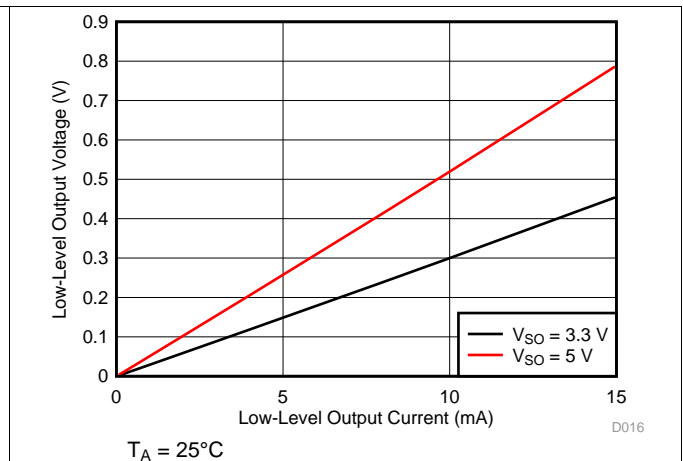


Figure 16. Low-Level Output Voltage vs Low-Level Output Current

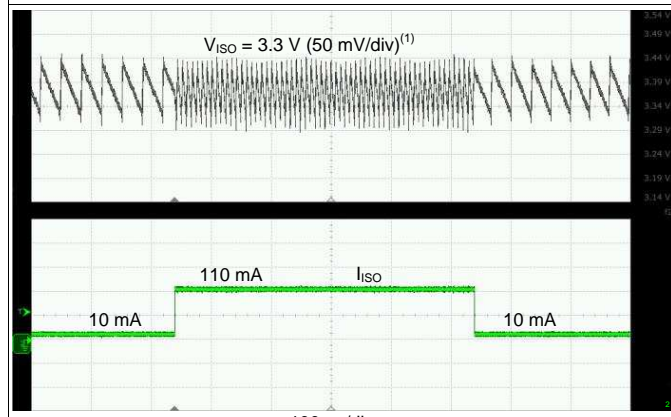


Figure 17. 10-mA to 110-mA Load Transient Response

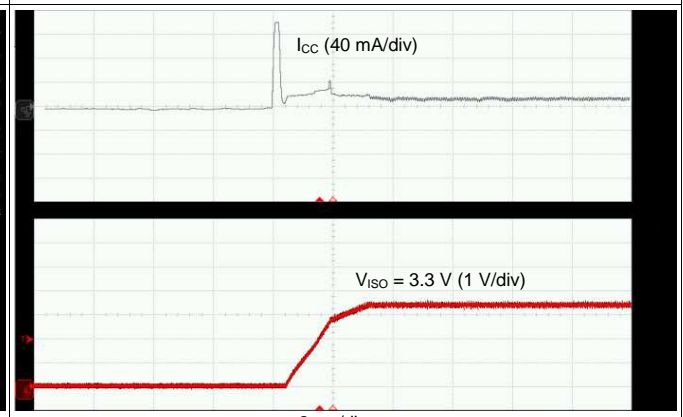


Figure 18. Soft Start at 10-mA Load

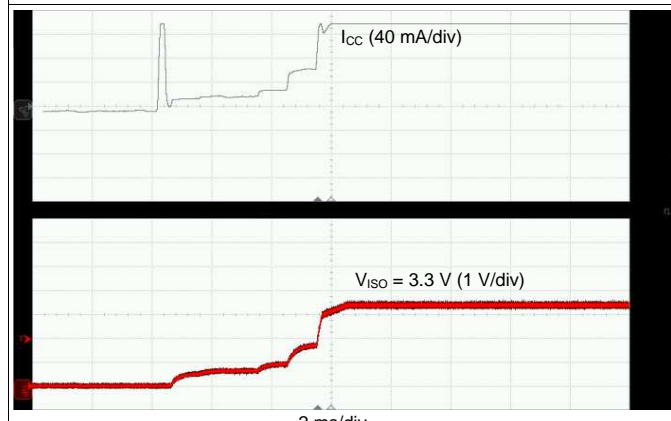


Figure 19. Soft Start at 120-mA Load

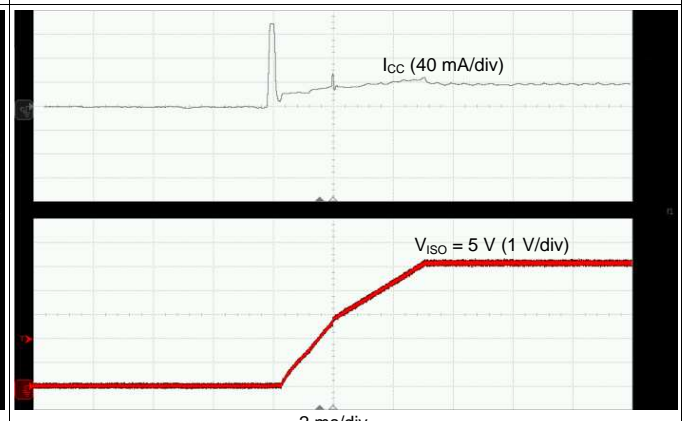
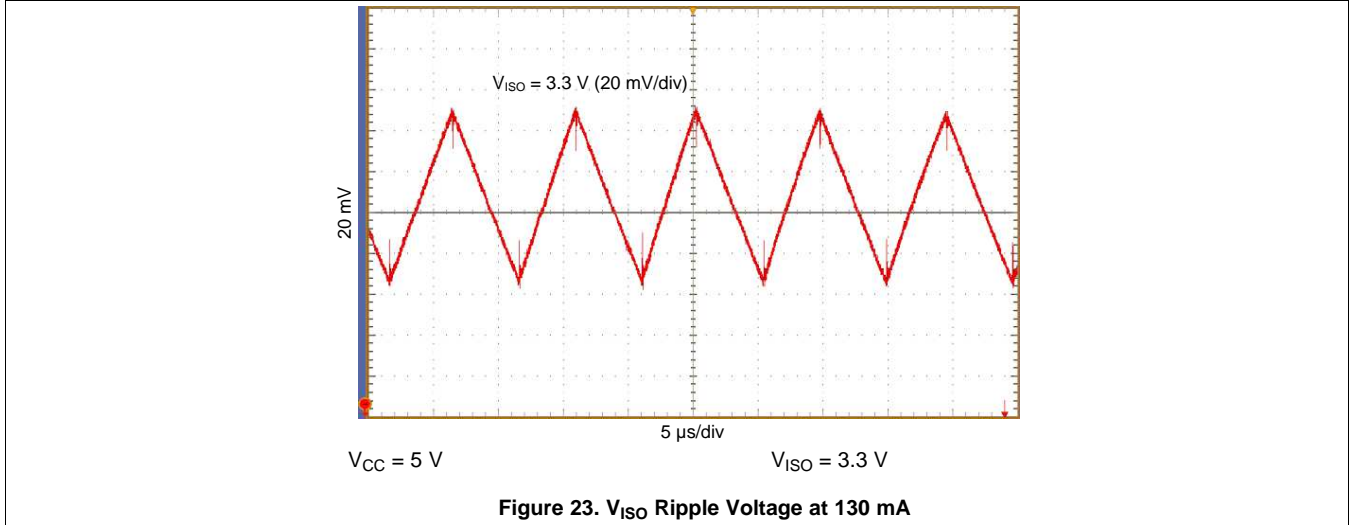
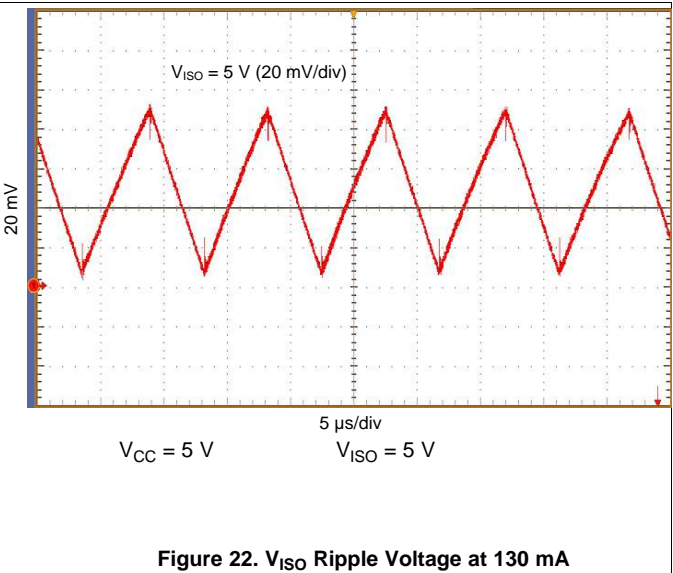
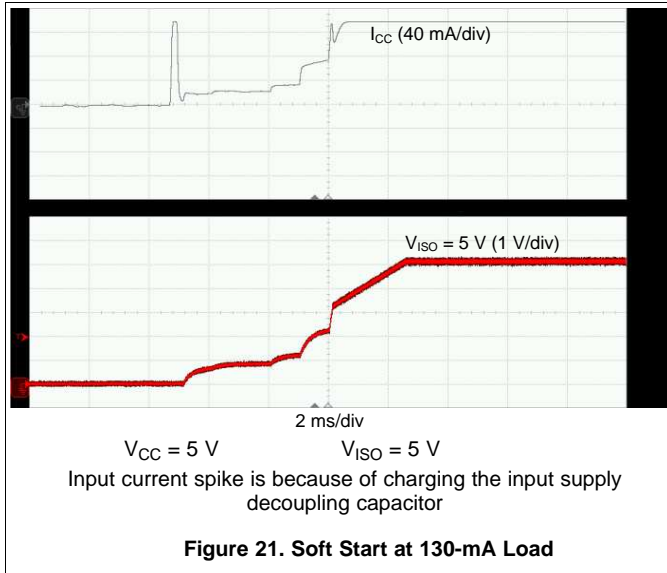
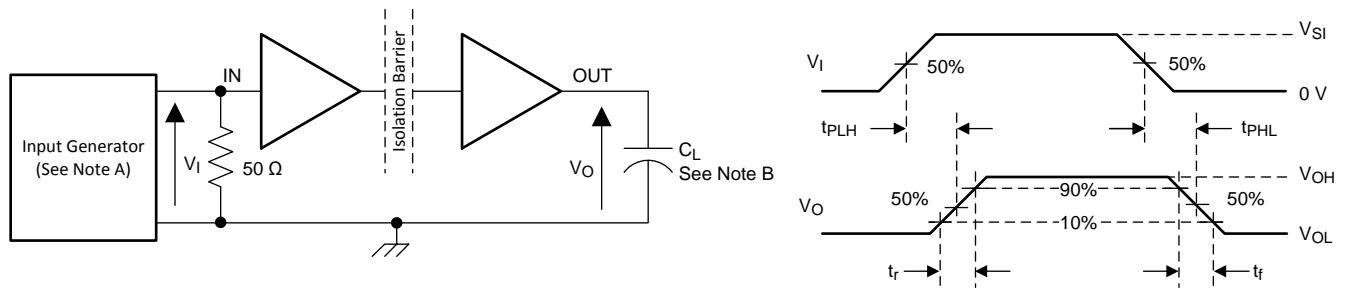


Figure 20. Soft Start at 10-mA Load

Typical Characteristics (continued)



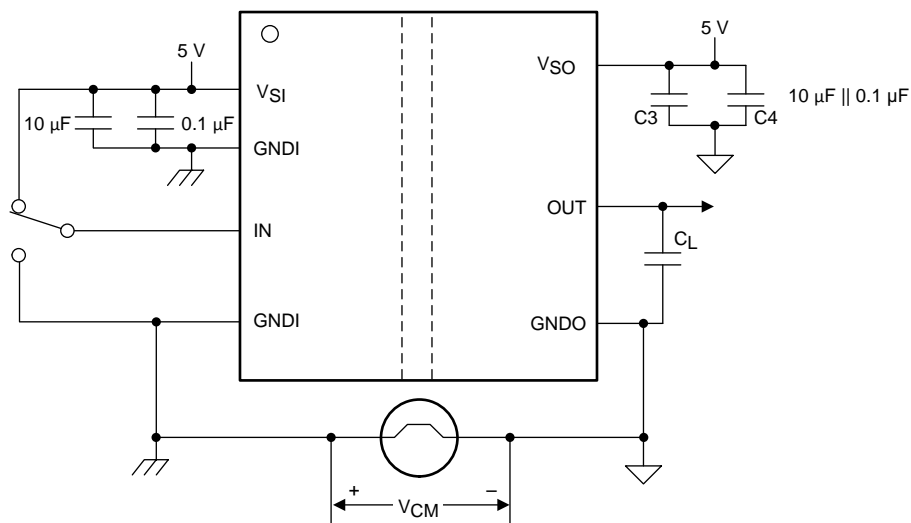
8 Parameter Measurement Information



The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50 \Omega$. At the input, 50- Ω resistor is required to terminate the input generator signal. The resistor is not required in the actual application.

$C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 24. Switching Characteristics Test Circuit and Voltage Waveforms



Copyright © 2017, Texas Instruments Incorporated

$C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Pass-fail criteria: Outputs must remain stable.

Figure 25. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ISOW784x family of devices comprises a high-efficiency, low-emissions isolated DC-DC converter and four high-speed isolated data channels. Figure 26 shows the functional block diagram of the ISOW784x family of devices.

The integrated DC-DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of a high-Q on-chip transformer provide high efficiency and low radiated emissions. The integrated transformer uses thin film polymer as the insulation barrier.

The V_{CC} supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified and regulated to either 3.3 V or 5 V, depending on the SEL pin. The output voltage, V_{ISO} , is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{CC} and V_{ISO} supplies which ensures robust system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

The integrated signal-isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. Figure 27 shows a functional block diagram of a typical signal isolation channel.

The ISOW784x family of devices is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

9.2 Functional Block Diagram

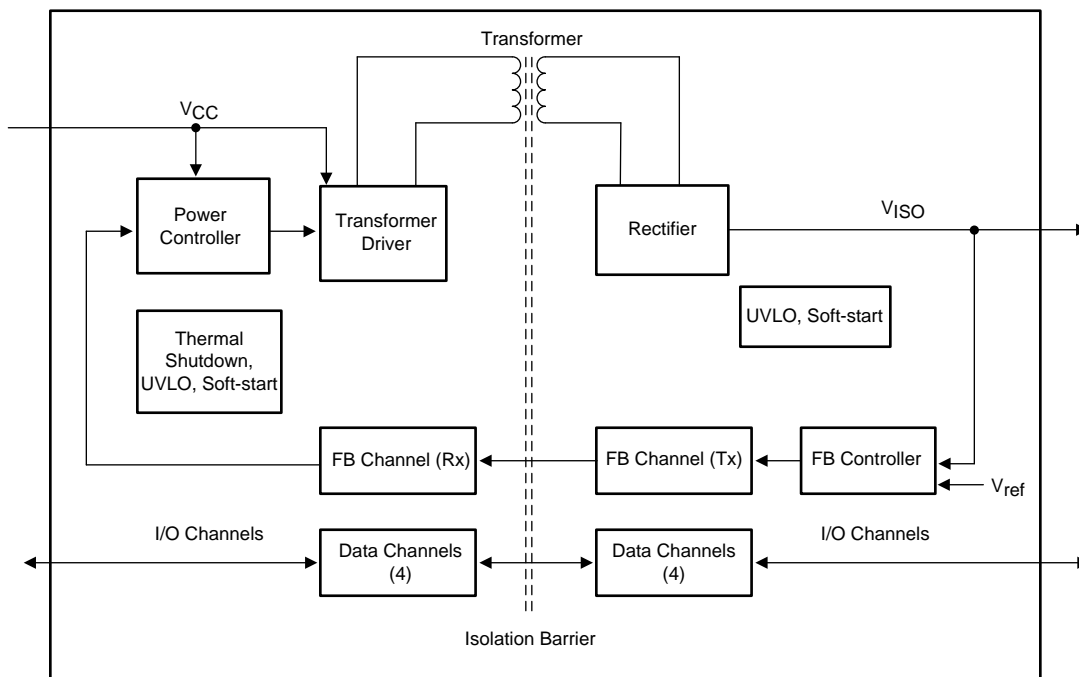
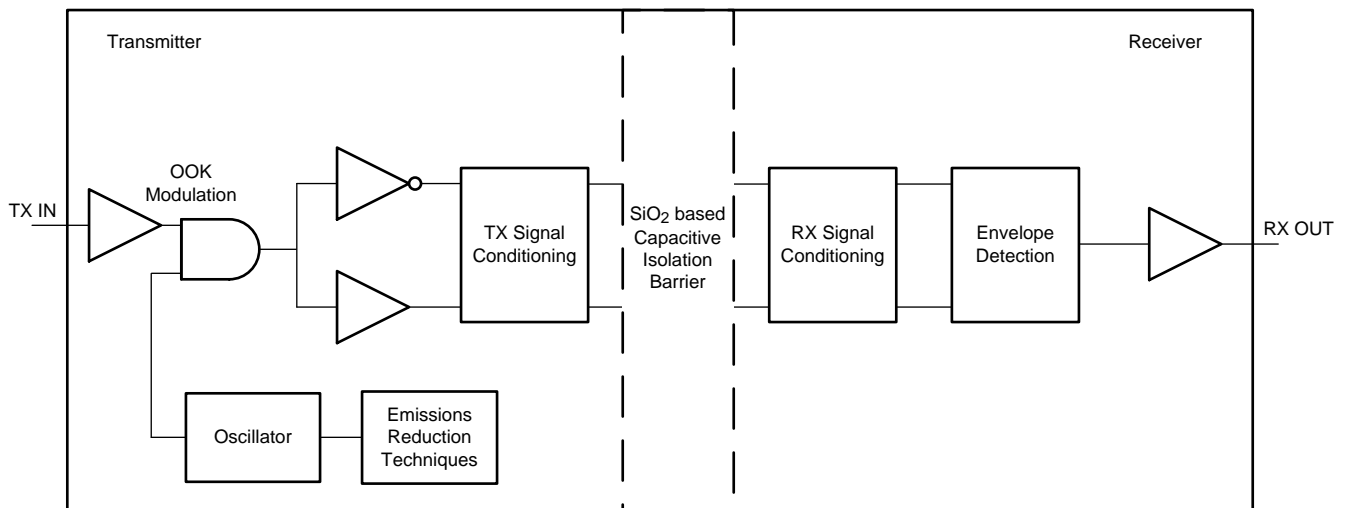


Figure 26. ISOW784x Block Diagram

Functional Block Diagram (continued)



Copyright © 2017, Texas Instruments Incorporated

Figure 27. Conceptual Block Diagram of a Capacitive Data Channel

Figure 28 shows a conceptual detail of how the OOK scheme works.

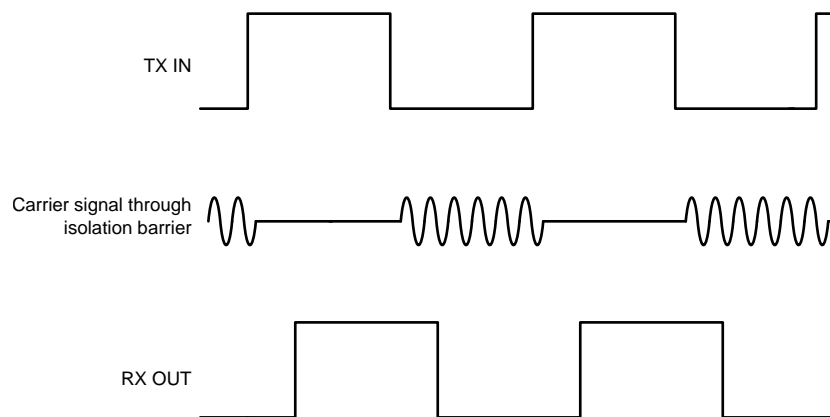


Figure 28. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

Table 1 provides an overview of the device features.

Table 1. Device Features

| PART NUMBER ⁽¹⁾ | CHANNEL DIRECTION | MAXIMUM DATA RATE | DEFAULT OUTPUT STATE | RATED ISOLATION ⁽²⁾ |
|----------------------------|----------------------|-------------------|----------------------|--|
| ISOW7840 | 4 forward, 0 reverse | 100 Mbps | High | 5 kV _{RMS} / 7071 V _{PK} |
| ISOW7840F | | | Low | |
| ISOW7841 | 3 forward, 1 reverse | | High | |
| ISOW7841F | | | Low | |
| ISOW7842 | 2 forward, 2 reverse | | High | |
| ISOW7842F | | | Low | |
| ISOW7843 | 1 forward, 3 reverse | | High | |
| ISOW7843F | | | Low | |
| ISOW7844 | 0 forward, 4 reverse | | High | |
| ISOW7844F | | | Low | |

(1) The F suffix is part of the orderable part number. See the [Mechanical, Packaging, and Orderable Information](#) section for the full orderable part number.

(2) For detailed isolation ratings, see the [Safety-Related Certifications](#) table.

9.3.1 Electromagnetic Compatibility (EMC) Considerations

The ISOW784x family of devices use emissions reduction schemes for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISOW784x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.3.2 Power-Up and Power-Down Behavior

The ISOW784x family of devices has built-in UVLO on the V_{CC} and V_{ISO} supplies with positive-going and negative-going thresholds and hysteresis. When the V_{CC} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{CC} supply and charges the V_{ISO} output in a controlled manner, avoiding overshoots. Outputs of the isolated data channels are in an indeterminate state until the V_{CC} or V_{ISO} voltage crosses the positive-going UVLO threshold. When the UVLO positive-going threshold is crossed on the secondary side V_{ISO} pin, the feedback data channel starts providing feedback to the primary controller. The regulation loop takes over and the isolated data channels go to the normal state defined by the respective input channels or their default states. Design should consider a sufficient time margin (typically 10 ms with 10-μF load capacitance) to allow this power up sequence before valid data channels are accounted for system functionality.

When V_{CC} power is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISO} capacitor then discharges depending on the external load. The isolated data outputs on the V_{ISO} side are returned to the default state for the brief time that the V_{ISO} voltage takes to discharge to zero.

9.3.3 Current Limit, Thermal Overload Protection

The ISOW784x family of devices is protected against output overload and short circuit. Output voltage starts dropping when the power converter is not able to deliver the current demanded during overload conditions. For a V_{ISO} short-circuit to ground, the duty cycle of the converter is limited to help protect against any damage.

Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the temperature goes above 180°C, thermal shutdown activates and the primary controller turns off which removes the energy supplied to the V_{ISO} load, which causes the device to cool off. When the junction temperature goes below 150°C, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the design to prevent the device junction temperatures from reaching such high values.

9.4 Device Functional Modes

Table 2 lists the supply configurations for these devices.

Table 2. Supply Configurations

| SEL INPUT | V_{CC} | V_{ISO} |
|-----------------------------|----------------------|----------------------|
| Shorted to V_{ISO} | 5 V | 5 V |
| Shorted to GND2 or floating | 5 V | 3.3 V |
| Shorted to GND2 or floating | 3.3 V ⁽¹⁾ | 3.3 V ⁽²⁾ |

(1) $V_{CC} = 3.3$ V, SEL shorted to V_{ISO} (essentially $V_{ISO} = 5$ V) is not recommended mode of configuration.

(2) The SEL pin has a weak pulldown internally. Therefore for $V_{ISO} = 3.3$ V, the SEL pin should be strongly connected to the GND2 pin in noisy system scenarios.

Table 3 lists the functional modes for ISOW784x devices.

Table 3. Function Table⁽¹⁾

| INPUT SUPPLY (V_{CC}) | INPUT (INx) | OUTPUT (OUTx) | COMMENTS |
|---------------------------|-------------|-----------------------------|---|
| PU | H | H | Output channel assumes the logic state of its input |
| | L | L | |
| | Open | Default | Default mode ⁽²⁾ : When INx is open, the corresponding output channel assumes logic based on default output mode of selected version |
| PD | x | Undetermined ⁽³⁾ | |

(1) PU = Powered up ($V_{CC} \geq 2.7$ V); PD = Powered down ($V_{CC} < 2.1$ V); X = Irrelevant; H = High level; L = Low level, V_{CC} = Input-side supply

(2) In the default condition, the output is high for ISOW784x and low for ISOW784x with the F suffix.

(3) The outputs are in an undetermined state when $V_{CC} < 2.1$ V.

9.4.1 Device I/O Schematics

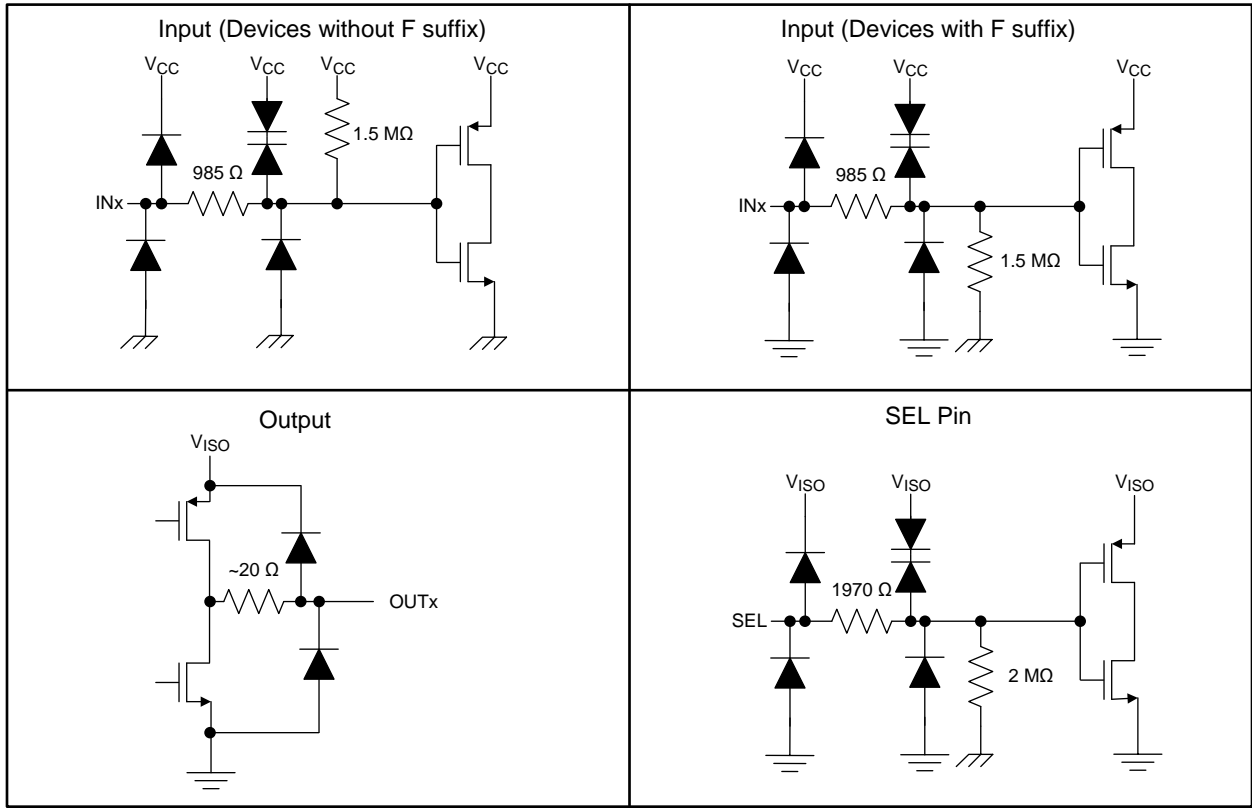


Figure 29. Device I/O Schematics

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

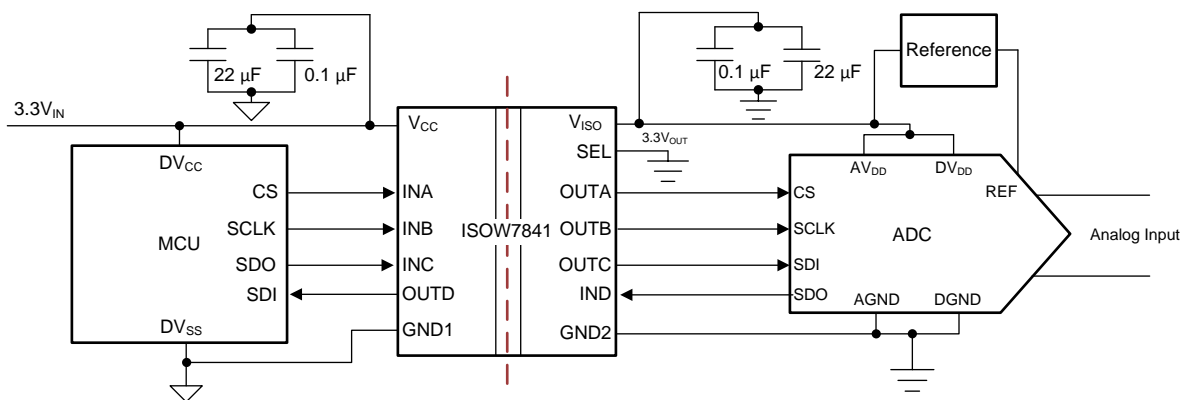
10.1 Application Information

The ISOW784x devices are high-performance, quad channel digital isolators with integrated DC-DC converter. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to the integrated DC-DC converter in ISOW784x, the isolated supply is generated inside the device that can be used to power isolated side of the device and peripherals on isolated side, thus saving board space. The ISOW784x devices use single-ended CMOS-logic switching technology. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is Microcontroller or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

ISOW784x devices are suitable for applications that have limited board space and desire more integration. These devices are also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

10.2 Typical Application

Figure 30 shows the typical schematic for SPI isolation.



Copyright © 2017, Texas Instruments Incorporated

Figure 30. Isolated Power and SPI for ADC Sensing Application With ISOW7841

10.2.1 Design Requirements

To design with this device, use the parameters listed in [Table 4](#).

Table 4. Design Parameters

| PARAMETER | VALUE |
|---|---------------------------|
| Input voltage | 3 V to 5.5 V |
| Decoupling capacitor between V_{CC} and GND1 | 0.1 μ F to 10 μ F |
| Decoupling capacitor between V_{ISO} and GND2 | 0.1 μ F to 10 μ F |

Because of very-high current flowing through the ISOW7841 V_{CC} and V_{ISO} supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10- μF capacitor is adequate, higher decoupling capacitors (such as 47 μF) on both the V_{CC} and V_{ISO} pins to the respective grounds are strongly recommended to achieve the best performance.

10.2.2 Detailed Design Procedure

The ISOW784x family of devices only requires external bypass capacitors to operate. These low-ESR ceramic bypass capacitors must be placed as close to the chip pads as possible.

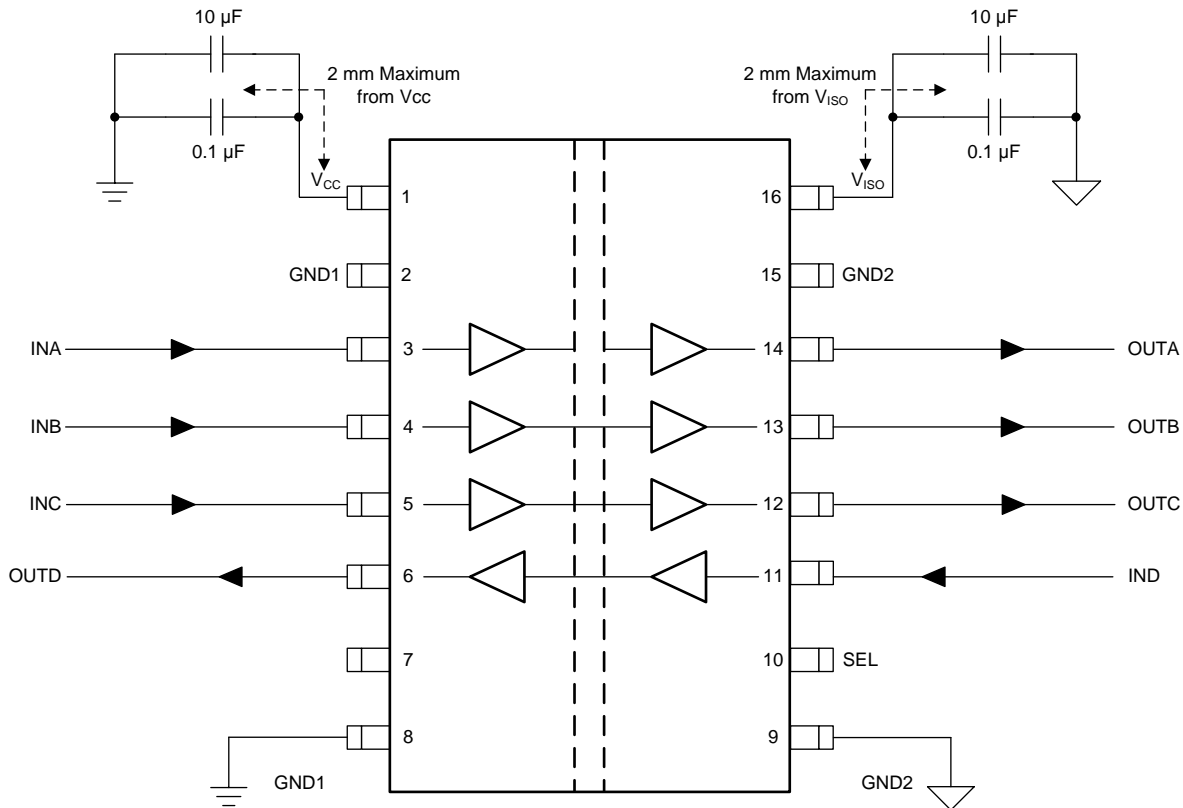


Figure 31. Typical ISOW7841 Circuit Hook-Up

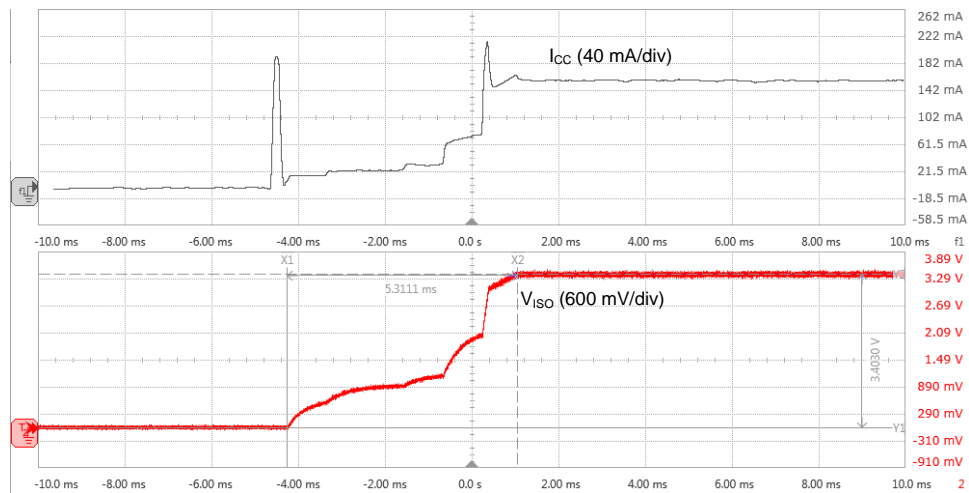
The V_{CC} power-supply input provides power to isolated data channels and to the isolated DC-DC converter. Use Equation 1 to calculate the total power budget on the primary side.

$$I_{CC} = (V_{ISO} \times I_{ISO}) / (\eta \times V_{CC}) + I_{inpx}$$

where

- I_{CC} is the total current required by the primary supply.
- V_{ISO} is the isolated supply voltage.
- I_{ISO} is the external load on the isolated supply voltage.
- η is the efficiency.
- V_{CC} is the supply voltage.
- I_{inpx} is the total current drawn for the isolated data channels and power converter when data channels are toggling at a specific data rate. This data is shown in the [DC Electrical Characteristics—5-V Input, 5-V Output](#) table. (1)

10.2.3 Application Curve



$$V_{CC} = 3.3 \text{ V}$$

$$I_{ISO} = 70 \text{ mA}$$

Input current spike is because of charging the input supply decoupling capacitor

Figure 32. Soft-Start Waveform

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. The input supply must have an appropriate current rating to support output load and switching at the maximum data rate required by the end application. For more information, refer to the [Detailed Design Procedure](#) section.

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low-EMI PCB design (see [Figure 33](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Keep decoupling capacitors as close as possible to the V_{CC} and V_{ISO} pins.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Because the device has no thermal pad to dissipate heat, the device dissipates heat through the respective GND pins. Ensure that enough copper is present on both GND pins to prevent the internal junction temperature of the device from rising to unacceptable levels.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.2 Layout Example

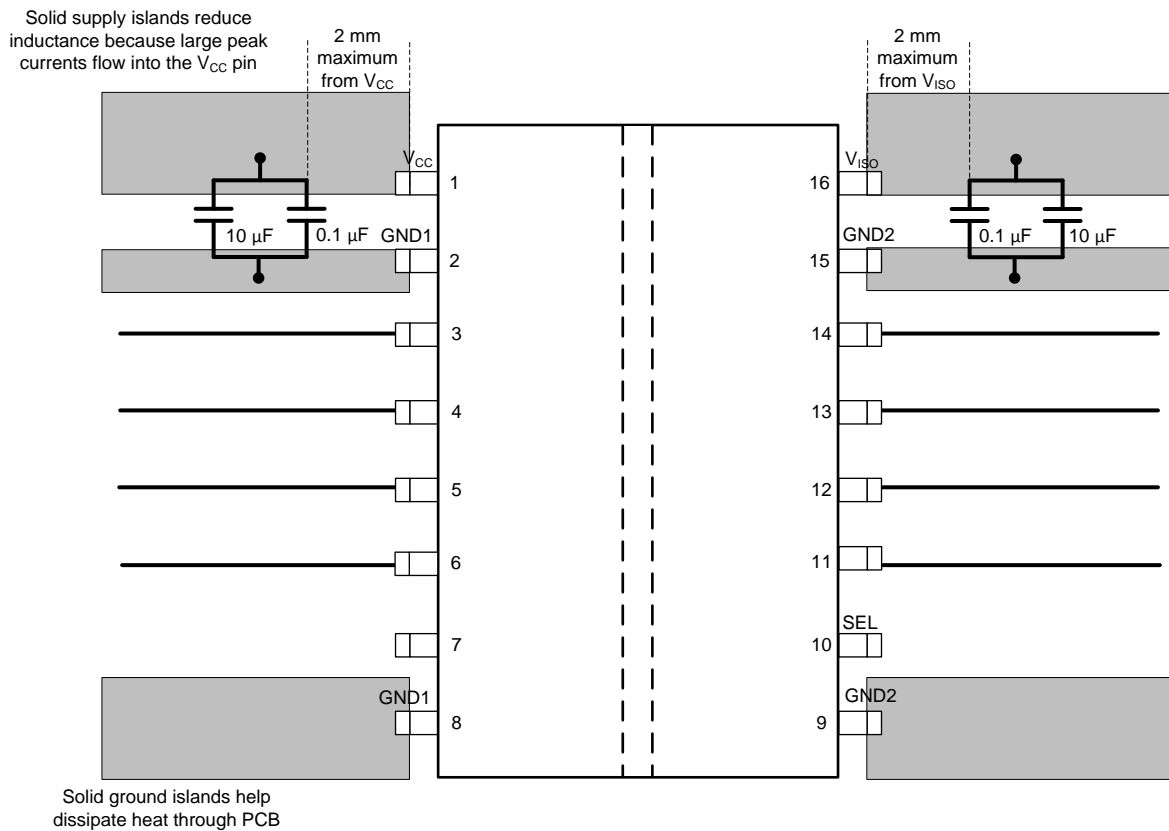


Figure 33. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- [Digital Isolator Design Guide](#)
- [Isolation Glossary](#)
- [ISOW784x Quad-Channel Digital Isolator With Integrated DC-DC Converter Evaluation Module](#)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| ISOW7840 | Click here | Click here | Click here | Click here | Click here |
| ISOW7841 | Click here | Click here | Click here | Click here | Click here |
| ISOW7842 | Click here | Click here | Click here | Click here | Click here |
| ISOW7843 | Click here | Click here | Click here | Click here | Click here |
| ISOW7844 | Click here | Click here | Click here | Click here | Click here |

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ISOW7840DWE | PREVIEW | SOIC | DWE | 16 | 40 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7840DWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7840FDWE | PREVIEW | SOIC | DWE | 16 | 40 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7840FDWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7841DWE | ACTIVE | SOIC | DWE | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISOW7841 | Samples |
| ISOW7841DWER | ACTIVE | SOIC | DWE | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISOW7841 | Samples |
| ISOW7841FDWE | ACTIVE | SOIC | DWE | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISOW7841F | Samples |
| ISOW7841FDWER | ACTIVE | SOIC | DWE | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISOW7841F | Samples |
| ISOW7842DWE | PREVIEW | SOIC | DWE | 16 | 40 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7842DWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7842FDWE | PREVIEW | SOIC | DWE | 16 | 40 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7842FDWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7843DWE | PREVIEW | SOIC | DWE | 16 | 40 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7843DWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7843FDWE | PREVIEW | SOIC | DWE | 16 | 75 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7843FDWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7844DWE | PREVIEW | SOIC | DWE | 16 | 40 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7844DWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7844FDWE | PREVIEW | SOIC | DWE | 16 | 40 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISOW7844FDWER | PREVIEW | SOIC | DWE | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



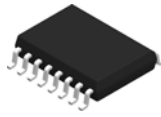
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISOW7841DWER | SOIC | DWE | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISOW7841FDWER | SOIC | DWE | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

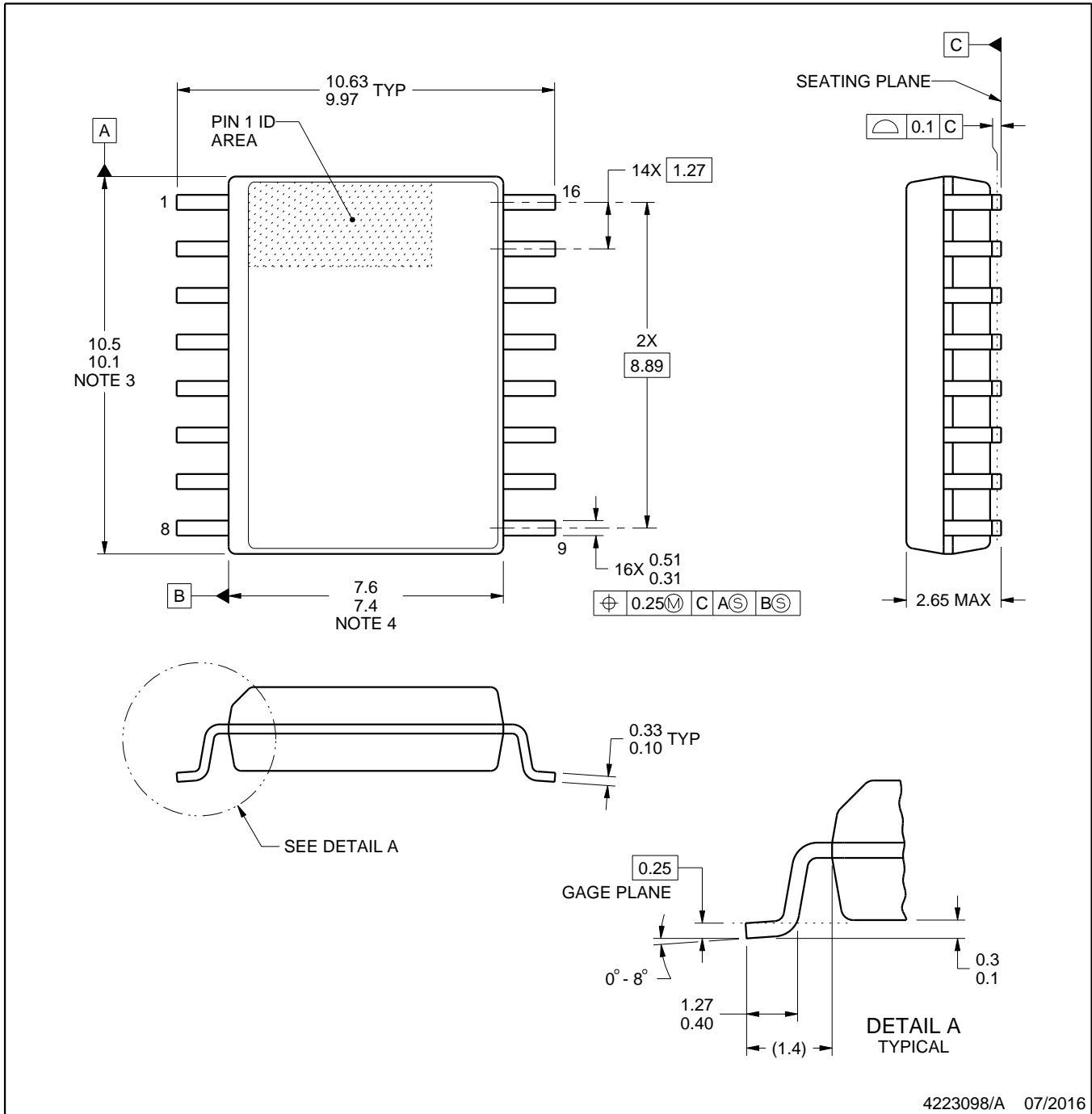
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISOW7841DWER | SOIC | DWE | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISOW7841FDWER | SOIC | DWE | 16 | 2000 | 367.0 | 367.0 | 38.0 |



DWE0016A

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



NOTES:

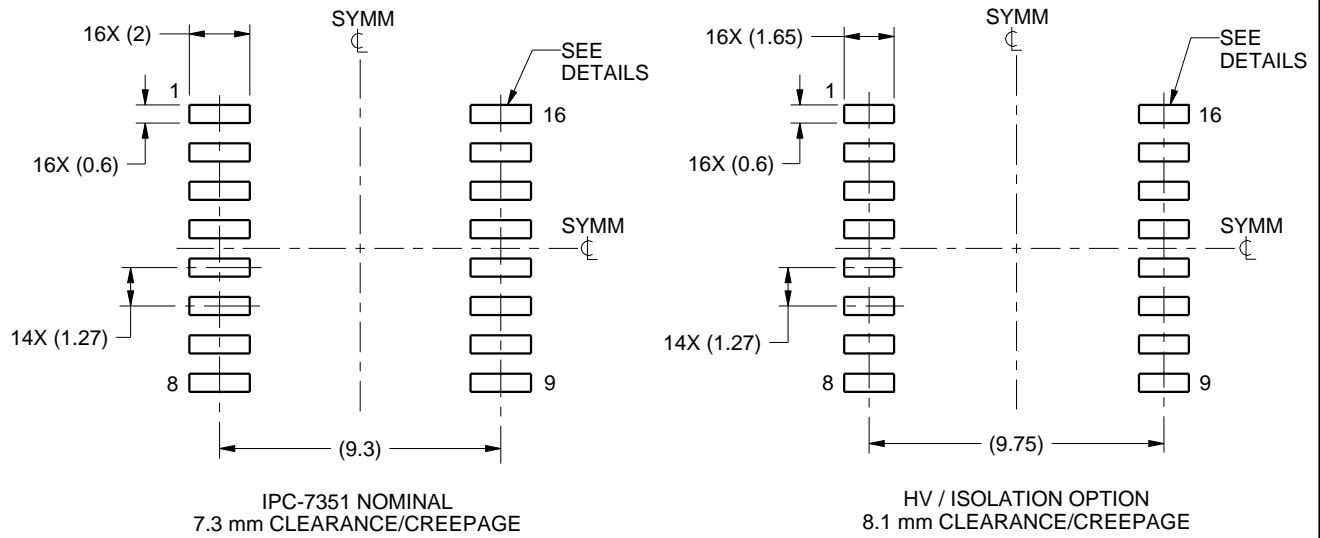
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

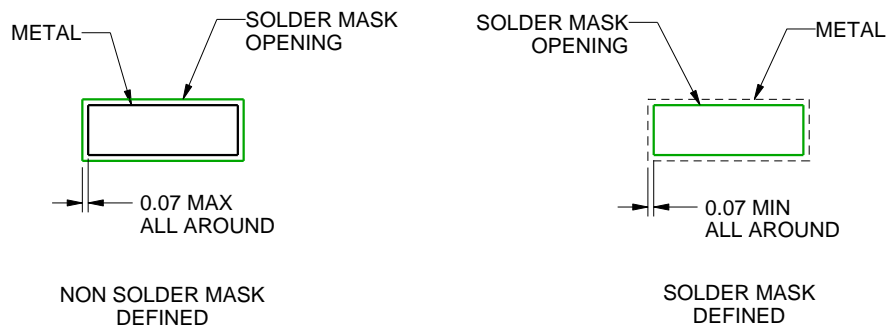
DWE0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

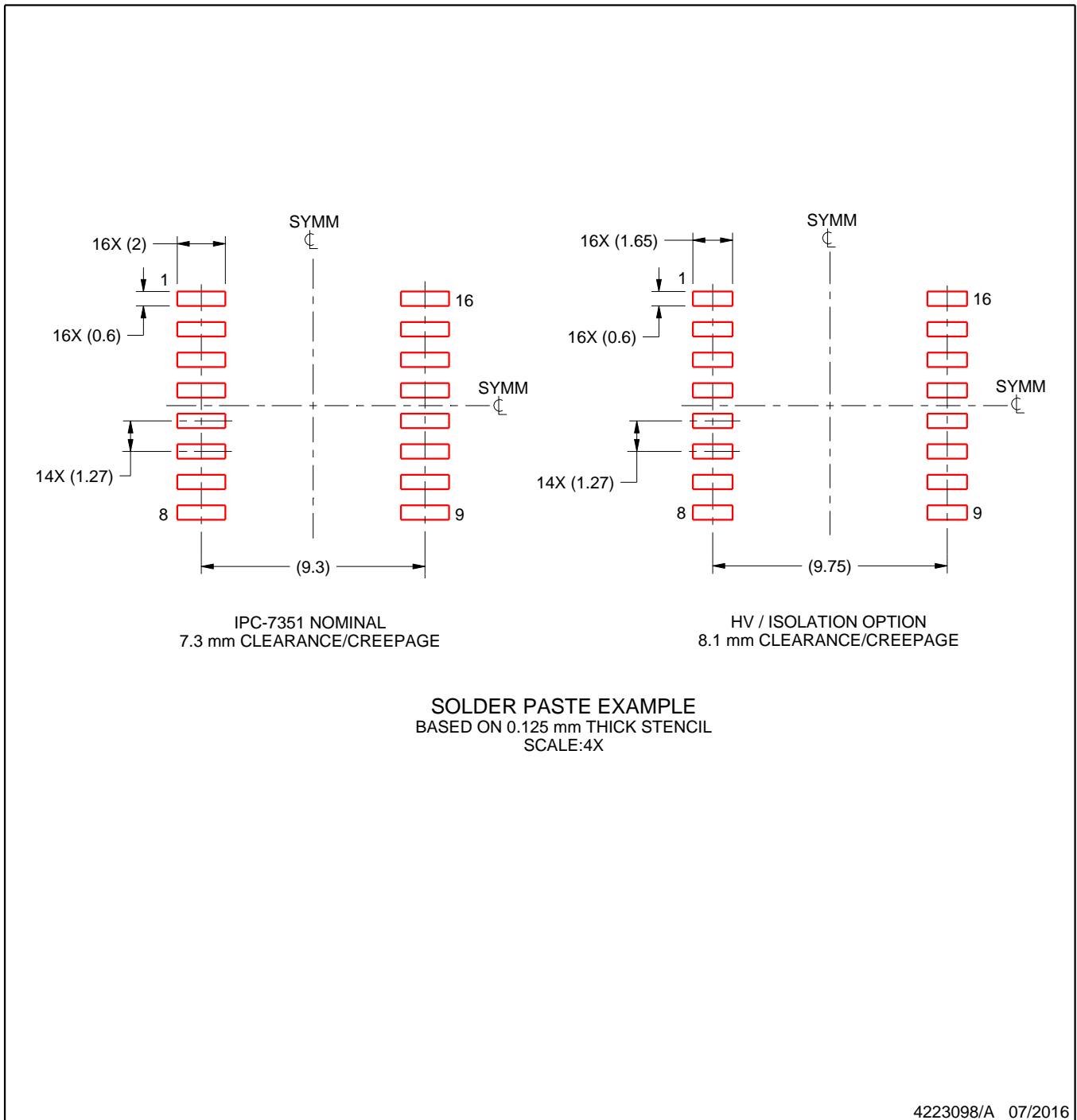
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated